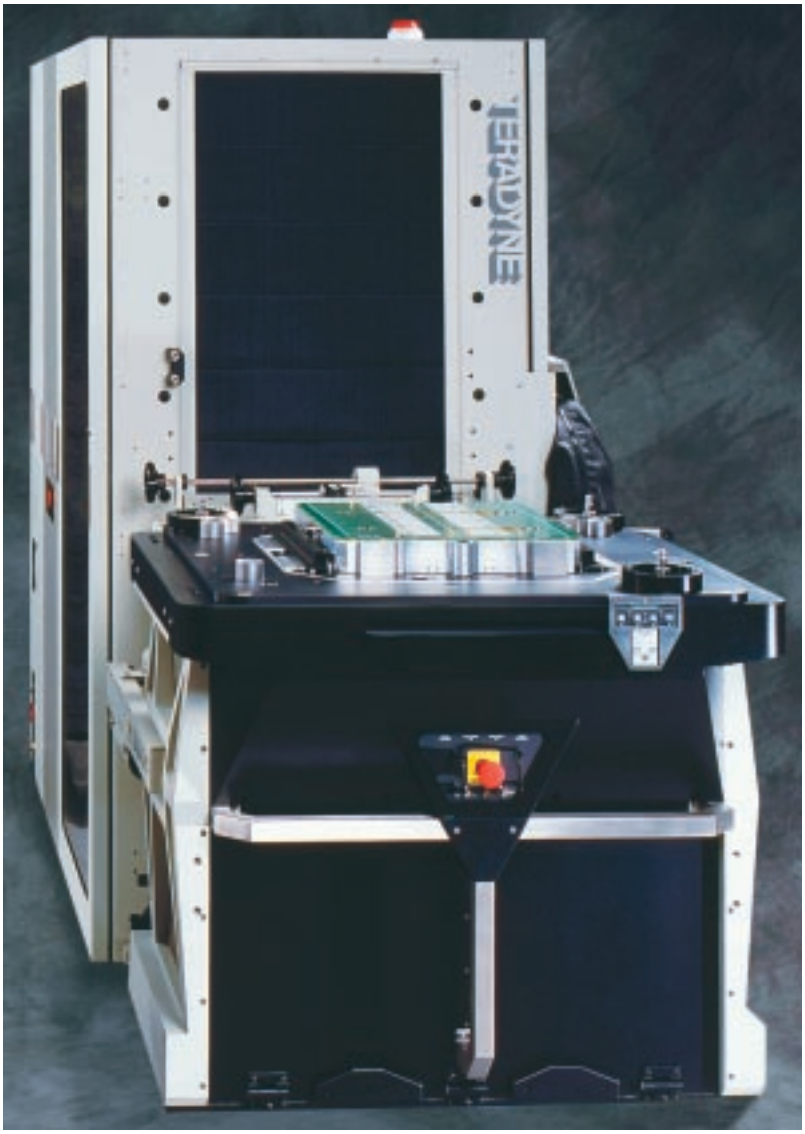
Integra FLEX

System Description



Disclaimers

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Executive Summary

Integra FLEX – Revolutionizing ATE Solutions

Device manufacturers are under increasing pressure to improve overall resource utilization and time-to-market to compete with the pace of technology change and falling device ASPs. This pressure is driving manufacturers to rethink the technology they purchase to manufacture and deliver their products to market. Whether Teradyne is working with Product Management, Test Engineering, or Device Manufacturing, they each share the economic goals of speeding overall device development time, improving utilization of equipment and resources, and providing the required performance to support device development and introduction.

Integra FLEX brings to the marketplace a ***revolution*** in mixed-signal multi-site test with a ***wide range*** of instrumentation to cover a wide variety of device segments – DFT to SOC. The architectural features of FLEX will exceed market expectations for delivering improvements in performance, productivity, quality and overall test costs. How customers think about ATE will never be the same as Teradyne introduces the FLEX features — *Universal Slot Architecture*, *TimeTracks*, *Background DPS*, *IG-XL 5.0 software*, *and Performance-on-Demand* — to provide device manufacturers with new degrees of freedom. It's what you would expect from the leader in ATE solutions!

Integra FLEX was designed to address the key cost priorities of our customers:*improving manufacturing utilization*, *increasing manufacturing capacity*, *and reducing time-to-revenue*.

Manufacturing Utilization

FLEX was designed with the explicit objective to improve manufacturing utilization of ATE. Teradyne's mechanical engineers designed the FLEX with the *Universal Slot Architecture* for configuration flexibility. Instrumentation teams designed Integrated Instruments to increase the available resources behind each pin and simplify the applications work required for device program development. Teradyne's *Performance-on-Demand model* for the FLEX provides real-time enabling of system functionality to better align required performance and device ATE costs. This "pay-per-use" model is an exciting feature developed in response to customer requests for more functional flexibility in Teradyne's ATE solutions.

FLEX introduces Teradyne's *Universal Slot Architecture*. The FLEX test head contains 24 universal slots, meaning that any instrument can go into any test head slot (any board, any slot), whether you need digital, AC, DC, microwave, DFT test capability. This feature provides customers with the flexibility to configure the FLEX to support a wide range of device testing needs (e.g., mixed-signal, standard analog, digital, uwave, etc.) with just one configuration. The FLEX is a *tester-in-a-test head architecture*. Unlike other test platforms, which have both a test head and mainframe components, the majority of FLEX instrumentation is contained on a single channel card that inserts into one of the test head slot of the FLEX.

Improvements in manufacturing utilization are also achieved through the *Integrated Instrumentation* of FLEX. Teradyne engineers have achieved never before seen levels of integration, providing unmatched capability behind each pin in the system. For example, FLEX offers per-pin PPMU on all instruments and *DIB Access*, which allows any pin to be connected to any instrument, without applications circuitry. The suite of DC instruments provides multiple TMU and differential voltmeters per instrument. FLEX digital instruments offer new levels of integration with self-contained MTO, multiple DSSC engines, and enhanced SCAN functionality. The result is a revolution in resource availability and flexibility to support the device testing needs of our customers.

Teradyne is also introducing its new *Performance-on-Demand* option on the FLEX system. This capability allows real time enabling of key system functionality (e.g., data rate, MTO, SCAN, LVM, DSSC, etc.). These on-the-fly performance features are licensed to match FLEX capabilities with the device test requirements to improve utilization and reduce associated test costs.

Manufacturing Capacity

Another key design objective of the Integra FLEX was to increase the manufacturing capacity of ATE by fundamentally enhancing architectural features to achieve new levels of throughput. This expanded throughput is enabled by the *Background DSP* and *TimeTracks* architectural features of the FLEX.

The *Background DS* architecture of the Integra FLEX removes test bottlenecks that limit the throughput

performance of other ATE platforms. While other systems have shared data movement and processing resources, the FLEX has three DSP tiers and point-to-point move buses to support your device test processing. Level 1 real-time processing is always available. Here the complete signal processing is executed in the host test computer. Level 2 real-time signal processing is accomplished by the addition of up to eight (8) modular *Real-Time Processors* to the Integra FLEX system. Once installed, these modules are dynamically brought online as the number of parallel sites increases. These are modular boards which plug into the two system support boards and are scalable and upgradeable, based on your device testing needs. Level 3 real-time signal processing is available on-board on a per-instrument basis. The FLEX also has point-to-point move buses that connect each instrument to the test head support boards. As you move to testing more sites and more complex SOC devices you need a tester which eliminates the shared resources of moving and processing test data. FLEX was designed to eliminate shared resources and drive substantial improvements in throughput.

Teradyne is also introducing the *TimeTracks* architecture that is based on distributed pattern controlled instrumentation. Each FLEX instrument has a Pattern Generator that enables multi-site concurrent test capabilities, multiple time domains and direct instrument setups that are executed independently by each instrument. Precision timing control provides improved test repeatability.

Time-to-Revenue

Device manufacturers are also looking to their suppliers to improve the time it takes to move from initial device concept to the release of the device to the end applications. FLEX *IG-XL 5.0* software offers device manufacturers new tools and capability to meet the increasing complexity of device technology. FLEX also leverages proven production integration solutions to simplify docking and integration into the production environment.

IG-XL 5.0 speeds test program development with reusable test program IP and zero-time parallel test.The reusable test program IP optimizes test programs developed by expert test engineers for the novice or junior engineer. Because *IG-XL 5.0* is pc-based, program development can be done anywhere, anytime.

Multi-site test program development has never been faster with *IG-XL 5.0* software. Test engineers can develop a single site program and almost instantly go to multi-site test. The user-friendly programming environment, combined with these ease-of-use features, allows test programs to be developed faster then ever before.

Conclusion

The expanding need to improve overall resource utilization and time-to-market will drive the market to the FLEX platform and enabling technology. These architectural features are unique and offer our customers the opportunity to recognize a competitive advantage over their competitors.

Product management, test engineering, and manufacturing technicians are being drawn to the FLEX with its improved device program development tools and opportunities to lower costs through higher overall ATE utilization.

Integra FLEX offers to the market higher levels of mixed-signal multi-site test with a range of instrumentation to cover the broadest range of device segments. Architectural features of the system will enable FLEX to exceed market expectations for performance, productivity, quality, and overall test costs.

Please refer to the individual sections within this System Description, as indicated in parentheses () for more detailed information on each of these critical architectural features of the FLEX.

- Integra FLEX Hardware Architectural Features (Sections 1 and 5)
  - Tester-in-The-Tester
  - Universal Slots
    - 24 slots accept any instrument – DC, AC, Microwave, or Digital
    - 22 Digital instruments maximum
  - Direct Digital Synthesis Optical Reference Clock
    - 29-bit DDS clock on every instrument – DC, AC, Microwave, and Digital; completely independent; referenced to common precision 100 MHz system reference; <1.0pp-billion frequency ratio accuracy; generate any required clock frequency to 36 atosecond resolution; timing and phase relationship across all domains precisely known
  - Redundant (Per) Instrument Functional Blocks Reduce Shared System Resources
    - 29-bit DDS clock on every instrument
    - Pattern Generator on every instrument; up to eight (8) PatGens per site; up to five (5) logical PatGens per system across multiple instruments – DC, AC, Microwave, and Digital
    - Parameter Set memory on every instrument
    - Instrument triggering from test pattern, another instrument, test computer, or DUT
    - Per pin measurement unit (DC and AC instruments)
    - DIB Access allows primary and secondary instrument to connect to same pin without DIB application circuitry or relays (any pin, any instrument)
    - One or more Time Measurement Units (DC instruments)
    - Dynamically assigned, multi-bank, capture memory
    - High-speed, back-end data Move Bus; instruments initiate data move without tester computer intervention; allows simultaneous data move and instrument setup and capture of next test data

- Multi-Source Instrument Control
  - All copies of instrument across all sites setup from single broadcast write command from test computer
  - Pattern-controlled analog instruments – setup commands within test pattern are executed by the analog instruments
- Three-Level Signal Processing
  - Dynamically allocates real-time signal processing power for Background DSP or other processing as instruments and sites are added
  - Level 1 – Level 1 real-time processing is always available. Complete signal processing is executed in the host test computer.
  - Level 2 real-time signal processing is accomplished by the addition of up to eight (8) modular Real-Time Processors to the Integra FLEX system. Once installed, these modules are dynamically brought online as the number of parallel sites increases.
  - Level 3 real-time signal processing is available on-board on a per instrument basis.
- Digital Capabilities for the SOC and DFT World
  - 200 MHz maximum operating speed
  - edge placement accuracy of ±250 ps
  - 64 Meg vector memory behind each pin
  - 48 single-ended pins or 24 differential pin pairs per board
  - 1,056 digital pins maximum
  - three drivers per pin — large swing, small swing, and 50 Ohm terminated
  - MTO capture memory is 24 M deep, with 2 M Fail Map Memory
  - MTO source and capture is 32 bits wide on a single board
  - 3 Gbits of SCAN data available for every 16 channels that can be configured in any way needed
  - SCAN Broadcast capability for parallel test economics and longer equipment lifetime
  - Digital Source and Capture (DSSC) provides serial or parallel data at 16 bits wide, with the ability to chain two DSSC blocks together for 32-bit operations
  - Six (6) DSSC engines per board
  - Fast keep-alive function
  - Two high voltage drive pins per board
  - DIB Access per four channels/pins
  - PMU per pin
  - per pin overvoltage/overcurrent protection that disconnects the pin electronics from the DUT on an alarm condition

• Integra FLEX Design Objectives

- Enhance Manufacturing Utilization (Section 2)
  - High level of resources behind each pin
    - per-pin PMU on all instruments
    - DIB Access, which allows any pin to be connected to any instrument, without application circuitry
    - one or more on-board Time Measurement Units on each DC instrument
    - on-board differential voltmeters on each DC instrument
    - dual pin high voltage driver on Digital instruments
    - self-contained Memory Test and Fail Map Memory on each Digital instrument
    - six (6) independent Digital Signal Source/Capture engines each with 128Mbit memory, per Digital instrument
    - 3Gbit, totally configurable, SCAN data per 16 channels/pins on Digital instruments
    - Keep-Alive function on each Digital instrument
    - three LFO/mixers on microwave instrument suite
    - on-board Real-Time processor on microwave instrument
  - Universal Slots/Configuration Flexibility
    - Any instrument, any slot
    - Single instrument suite can be configured that will test the majority of devices in a product mix
    - A multi-site (e.g. quad) test DIB for a single device (e.g. a mixed-signal SOC) can be used on test systems configured not only for that mixed-signal SOC device, but on Integra FLEX test systems configured primarily for linear or digital/SOC devices, with a reduction in the number of sites (i.e. dual versus quad)
  - Performance On Demand (Section 2)
    - On-the-fly performance and feature licensing to match Integra FLEX capabilities with device test requirements
    - IG-XL 5.0 software tools
    - Hardware capabilties
    - DFT configuration
- Increase Manufacturing Capabilty (Section 2)
  - Elimination of Test System Bottlenecks
    - Non-pipelined test computer/test system link
    - Dynamically allocated, three-level Background DSP/Real-Time Processing
    - Instrument-initiated capture data moves on independent data Move Bus
    - Universal instrument slots provide unprecedented test head configuration flexibilty
    - Minimized shared test system resources
    - DIB access connects any pin to any instrument without DIB application circuitry or relays
  - Pattern controlled analog instruments
    - Instrument setups executed directly by instruments
    - Precision timing control provides improved test repeatability
- Improve Time-To-Market (Section 3)
  - Unrestricted test development (Section 4) – fully leverage test development
  - TimeTrack™ precision cross-domain debugging allows events from all instruments – DC, AC, Microwave, and Digital – to be precisely lined up (within 36 atoseconds) for rapid debug
  - Integrated tools support design-to-test pattern translation, test simulation, and DFT (Section 4)
  - Simplified docking and production integration – Catalyst and J750 prober/handler interface investments are fully protected and Integra FLEX compatible

• Multi-Level Test Development: IG-XL 5.0 Environment Features (Section 4)

- Key Objectives
- Extend the J750 IG-XL 5.0 software to provide a common platform for the entire Integra family of general-purpose testers
  - Provide a multi-level programming capability to accommodate a diverse development environment, and enable a shorter development time
  - Provide an advanced linear and mixed-signal use model and toolset to build on the DUT-centric test development environment of IG-XL 5.0

- General Programming Approach
  - Device data entry into enhanced spreadsheet
  - Seamless graphical interface and code-based programming
  - Test templates, elements, and procedures library
  - Immediate feedback on device parameters and timing relationships definitions
  - HTML help documentation generation
  - Design once, re-use many times
  - Standardized, familiar interface consistent with industry practice
- Procedure Development Environment
- Test Instance Editor
- Standard Test Templates
  - Functional (BIST, SCAN)
  - Pin PMU/Board PMU (DC parametrics)
  - Power Supply (ICC, Iddq)
  - A/D and D/A Converter (Diff. Lin., Int. Lin, Offset Error, Absolute Error)
  - MTO Embedded Memory
  - Test Debug Environment
  - WaveDesigner
  - WaveScope
  - Mixed-Signal Workshop
  - Native Multi-Site Capabilities
  - Multi-site testing is assumed
  - Valid test program for first site (Site0) is site neutral
  - Sites added by duplicating Tester Channel column and assigning instrument resources to correct channels
  - Built-in support for up to 32 sites with 90+% efficiency
- Virtual Test
  - VX Test Simulation Software
  - Digital VX – single seat license included with Integra FLEX
  - Mixed-Signal VX
  - qVX
  - DataScope
- Integrated Design-to-Manufacturing Support

Section 1

Integra FLEX
Overview

Integra FLEX Objectives

Teradyne's objectives for the Integra FLEX test system were to:

- Increase manufacturing capability 1) by maximizing **test system throughput** through the elimination of test system bottlenecks relative to the movement and processing of captured data and test instrumentation setup, 2) by the minimization of shared resources, and 3) by providing performance on demand for all aspects of the test system.
- Improve time-to-market 1) by providing a test **development environment that provides a set of seamless tools** suitable for both novice and experienced test programmer alike, that maximizes test development efficiency and re-use, 2) by providing a system that assumes multi-site parallel test, in both its hardware and software architectures, 3) by fully integrating the necessary EDA, VX, and DFT tools, and 4) by leveraging the proven solutions and prior customer investment in existing prober and handler interfaces.
- Provide a single, scalable test platform that would deliver the lowest cost-of-test solution for both 1) functional testing of devices ranging from linear to mixed-signal and microwave SOC, and 2) driving DFT techniques for digital and SOC devices, using the same software and instrument suite.
- Enhance manufacturing utilization by 1) providing the flexibility to be configured simply and quickly to accommodate changes in device mix, emergency situations, and new device technologies, and 2) enable peaks in device test demand to be accommodated with the existing mix of test system configurations on the test floor, with no reconfiguration.

Figure 1-1: Integra FLEX test system

Architectural Feature Overview

Prior to presenting how the Integra FLEX addresses each of these objectives, it is first appropriate to understand the key features of the Integra FLEX system and how they interact.

Tester-In-The-Testhead

The Integra FLEX system has a very small footprint that is achieved by eliminating equipment bays external to the test head, and integrating the manipulator and an auxiliary equipment cabinet into a single unit. The test head itself ***is*** the tester. With the exception of the test computer, all of the instruments are contained within the test head. As device test requirements evolve to accommodate more complex devices, such as wireless/RF SOC devices, microwave instruments can be added to the test head and the associated frequency synthesizers may be installed in the auxiliary cabinet. An IEEE bus is integrated into the Integra FLEX so that IEEE instruments may be added to the auxiliary cabinet as well and connected to the Integra FLEX system as

needed. This modular, self-contained architecture eliminates unnecessary infrastructure costs for instruments or test capability that isn't needed. The test head is air-cooled, which eliminates the need for water cooling equipment and its attendant requirements. Figure 1-1 is a photograph of the complete Integra FLEX test system, while Figure 1-2 illustrates the footprint of the Integra FLEX system.

Universal Slots

The Integra FLEX supports any instrument — DC, AC, Microwave, or Digital — in any slot in the test head. Each instrument provides its own instrument-specific signal terminations appropriate for that instrument. This allows the test head to be configured without making tradeoffs relative to multi-site DIB support, provides significant improvements in signal routing flexibility, and allows rapid reconfiguration, regardless of whether instruments are removed, added, or repositioned. The test head can accommodate up to the maximum of 24 instruments (22 digital instruments maximum). The low cost universal slot test head and instrument suite of the Integra FLEX allow it to be economically configured to match varying DFT test insertion requirements across customers and the spectrum of devices deploying DFT techniques. As needs and technical requirements evolve, DFT-focused configurations of the Integra FLEX can be scaled to higher performance levels, including digital and mixed-signal functional test.

Mixed-Signal Clock Architecture

Clock architectures typically rely on a master frequency synthesizer with 1 Hz resolution that is divided by a series of integer dividers to generate divide-by-N and divide-by-X clock signals for driving the Device Under Test (DUT). These two clock signals are coherent and perfectly related to one another by an integer value. The inherent problem with this approach is that division by something other than an integer value isn't possible, and, as the reference frequency increases, the difference between division by two successive integers also increases, resulting in loss of resolution. Further, it is the ratio of F_{TEST} and F_{CLOCK} that must be precisely defined so that test time is minimized, accuracy and repeatability are as high as possible, the device specifications are met, and ultimately, all four of these factors are satisfied, preferably without compromise.

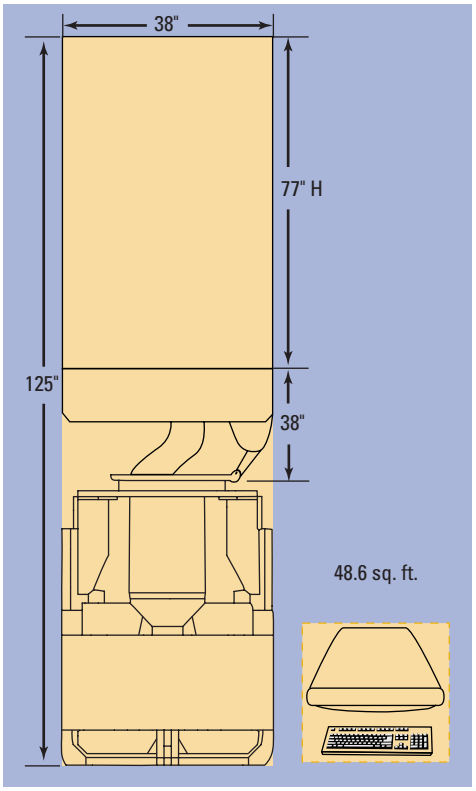


Figure 1-2: Integra FLEX footprint

To accommodate the needs of analog, digital, and mixed-signal testing in varying test environments, the Integra FLEX clock architecture allows the test engineer to find the optimal combined solution for minimum test time, highest possible measurement accuracy, and lowest possible repeatability errors, with no compromise in device specifications. Integra FLEX represents the fourth generation of clock architecture utilizing an Optical Reference Clock per instrument. Every instrument has its own 29-bit Direct Digital Synthesis Optical Reference Clock. The 29-bit clock provides <1.0pp-billion frequency ratio accuracy. Any required clock frequency can be generated, with a resolution of 36 atoseconds. The clock on each instrument is completely independent from those on other instruments so that individual instruments can run asynchronously with respect to each other, yet all clocks are referenced to a common precision 100 MHz system reference clock. This allows all instruments — DC, AC, Microwave, or Digital — to be fully time synchronized to one another. The Mixed-Signal Workshop tool is provided that enables the test engineer to set the device specifications and to know what the limits of tester performance

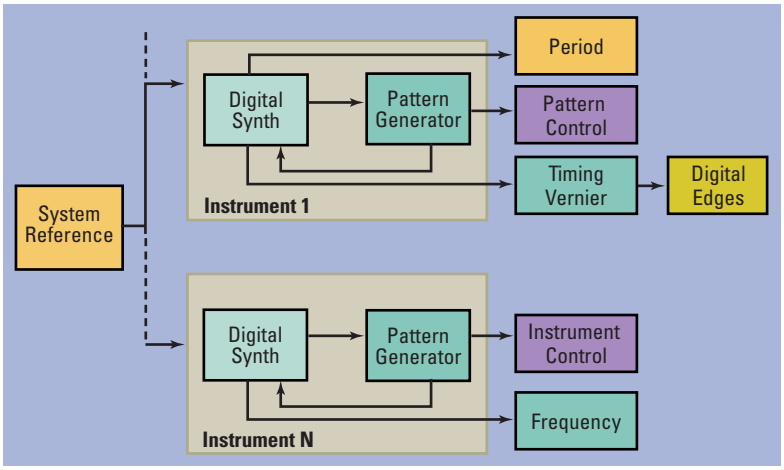


Figure 1-3: Integra FLEX DDS Optical Clock Reference architecture

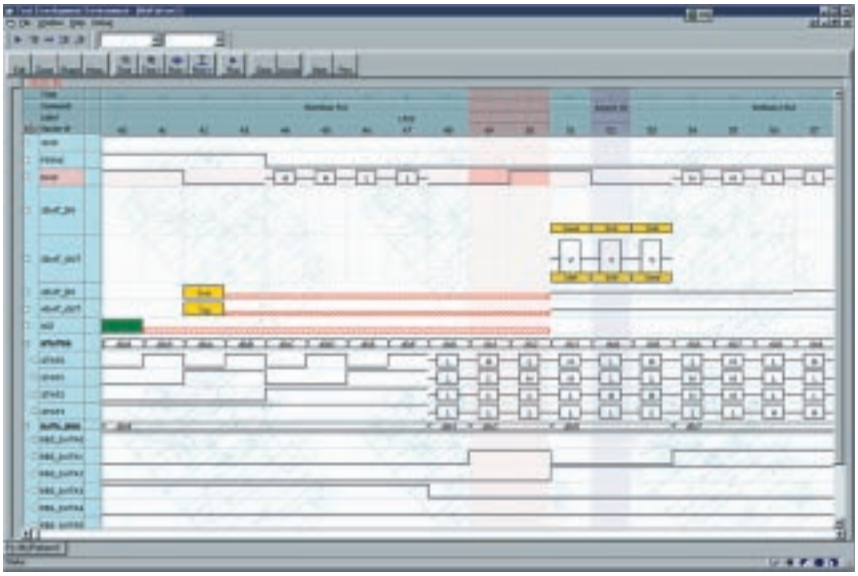


Figure 1-4: Time domain tool — synchronized analog and digital events

will be, ***before*** any tests are run. This has a significant impact on mixed-signal device testing, and can benefit digital and linear testing through improved clock accuracy and event synchronization as well.

With a clock on every instrument, timing and events can be very accurately controlled across all instrumentation. Because each clock is essentially a 29-bit counter synchronized to the master system reference, and with all starting at "zero" at t_0, the timing relationships among all clocks (instruments) are precisely known from one clock "tick" to the next, throughout every test. The time and phase for all instruments — DC, AC, Digital, or Microwave — can therefore be accurately tracked. A time domain tool is provided which allows the test engineer to look at all analog and digital events together, with resolution of all timing relationships to 36 atoseconds. This significantly reduces the effort required to debug test programs, and increases test repeatability from run to run and test system to test system. Refer to Figure 1-4.

Instrument Control

Test Computer/TCIO Bus

Each instrument receives test instructions, timing, parameter set data, and other test execution data from the test computer through the Teradyne-proprietary TCIO bus. All copies of an instrument across all sites can be triggered through the TCIO bus in a broadcast mode using a single write command. This could be used, for example, to trigger 20 V/I meters each on four DC instruments, and would result in 80 simultaneous measurements, under test program control, from a single instruction.

Pattern-Controlled Analog Instrumentation

Integra FLEX achieves significant improvements in test repeatability and throughput by enabling analog instrument control directly from the test pattern. All Integra FLEX instruments — DC, AC, or Microwave — have their own independent, on-board Pattern Generator, parameter set (Pset) memory, and as discussed previously, Direct Digital Synthesis Optical Reference Clock. Instrument setups are stored locally in the Pset memory on each instrument. As the pattern is executed on each analog instrument, instrument setup instructions embedded in the pattern are executed directly by the instrument, under precise timing control of the pattern. This significantly improves test repeatability, due to the precise timing control of the instruments from the pattern and their synchronization, and reduces test execution time, since instrument setup commands execute locally from Pset memory, and need not be transmitted from the test computer each time they are required. Refer to Figure 1-5.

Multi-site Concurrent SOC Test

The Integra FLEX test system is designed to fully support multi-site concurrent SOC test when it is configured to do so. Several inherent test system and instrument features contribute to that capability, either individually, or in combination. (For detailed information on the capability of each instrument, please refer to *Section 5: Instrument Description and Specifications*.)

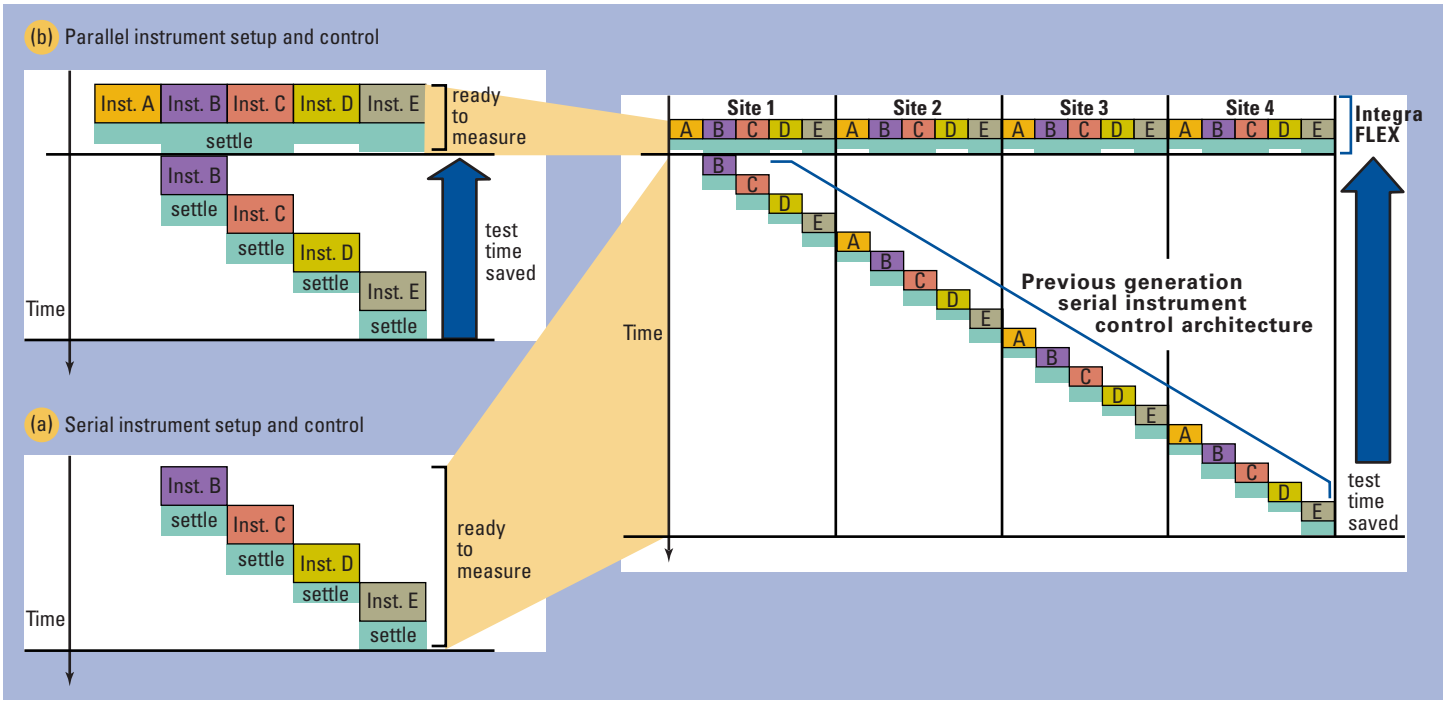


Figure 1-5: Integra FLEX pattern-controlled instrumentation setup

Direct Digital Synthesis Clock Per Instrument

As already described, every instrument has its own on-board 29-bit Direct Digital Synthesis Optical Reference Clock, which allows any required clock frequency to be generated, with a resolution of 36 atoseconds. Because the clock on each instrument is completely independent from those on other instruments, individual instruments can run asynchronously with respect to each other, yet all clocks are referenced to a common precision 100 MHz system reference clock. This allows all instruments — DC, AC, Microwave, and Digital — to be fully time synchronized to one another. This synchronization across instruments and sites, fully supports multi-site, concurrrent SOC testing.

Pattern Generator Per Instrument

As discussed previously, each instrument — DC, AC, Microwave, and Digital — has its own Pattern Generator (PatGen) on board driven from the instrument's clock subsystem. The PatGen controls local events and instrument setups. This means that all instruments, ***including analog, are controlled from the pattern***. Patterns can therefore exercise any device, not just digital. Each instrument can run asynchronously, at an independent rate dictated by the IP core within the DUT it is to test, yet all patterns are synchronized because the instrument clocks themselves are synchronized. This capability allows the Integra FLEX to concurrently test multiple IP cores, and their interactions, under actual device operating conditions.

Up to eight (8) instruments can be combined to form a logical PatGen. Up to five (5) logical PatGens can be configured at any given time within the Integra FLEX test system. Logical PatGens can be configured across individual DUTs or multiple sites, easily accommodating test requirements as they evolve or shift abruptly.

Pattern-Controlled Analog Instruments

As described earlier, the Integra FLEX analog instruments — DC, AC, and Microwave — can be directly controlled from the pattern executed from the on-board Pattern Generator. Instrument setups and commands embedded within the test pattern provide precisely controlled, synchronized and repeatable execution of concurrent testing across all instruments. This concurrent test capability extends from all instruments on a single site, to all instruments across multiple sites.

Instrument Triggering

Integra Flex instrument architecture is such that captures or measurements can be initiated through any one of four sources – from the test computer, from the test pattern, from another instrument, or from the DUT

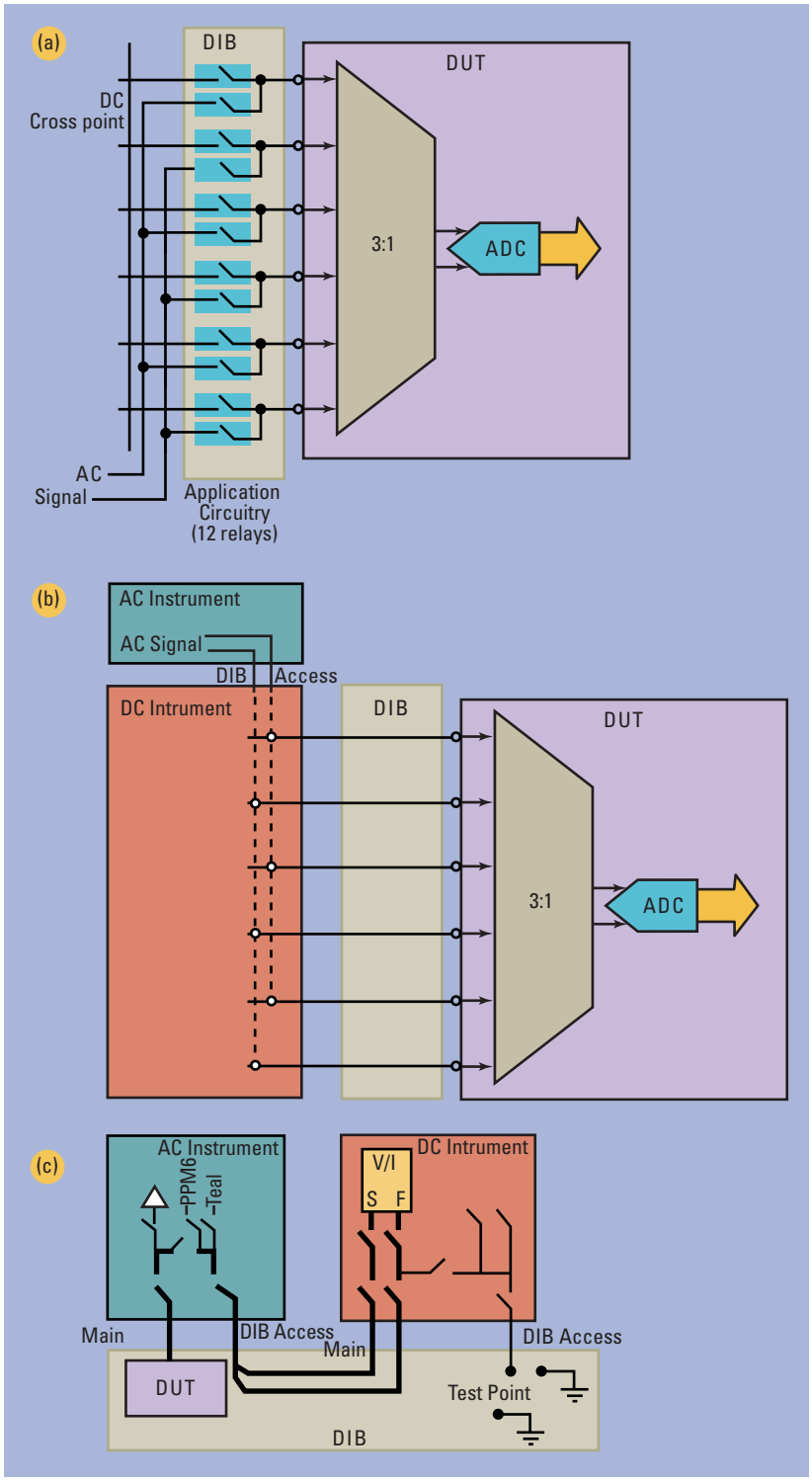


Figure 1-6: DIB Access

itself. Using the DIB Access feature (refer to following section) available on all instruments, instruments can "listen" to a variety of signal sense lines for capture/measurement triggers. This capability provides significant closed-loop testing abilities that enables rapid multi-site, concurrent device testing.

Per Instrument PPMU

DC, AC, and Digital instruments provide PPMU functions for parallel test of continuity and leakage.

Multiple Time Measurement Units

Every DC instrument has one or more Time Measurement Unit (TMU) subsystems. The TMU provides a means to tag DUT or instrument events with a very precise digital count referenced to another event. Each TMU has its own memory. The TMU 1) can look for events from the test pattern, 2) can be gated from the test pattern (i.e. "only look for events within this window"), 3) from any instrument, or 4) can accept events from the DUT itself. By providing all DC instruments have at least one TMU, parallel multi-site tests can be performed for rise/fall times, propagation delay, pulse width, frequency, and period.

DIB Access

DIB Access provides the ability to route signals from one instrument to another, without requiring DIB application relay circuitry. The DIB Access feature also provides a modulation input for the DC instruments so they can be driven from the AC instruments for high power modulated source requirements. To illustrate how DIB Access works to reduce the amount of DIB circuitry required, consider the case of a DUT consisting of an ADC with a 3:1 differential multiplexer front-end Refer to Figure 1-6.

If we assume the test requirement is to measure DC resistance on all six input lines, and then inject an AC signal to all three differential inputs through to the ADC for analysis, Figure 1-6(a) depicts the application circuitry required to perform this test without the Integra Flex DIB Access feature. Twelve relays are required on the DIB to route the AC signal source to the each of the differential inputs to the multiplexer. Figure 1-6(b) shows how the relays are no longer required in the same test situation in the Integra Flex test system. The AC signal source is routed from the AC instrument to the DC instrument(s) within the instrument DIB Access subsystem(s), reducing the amount of application circuitry and the effort required to design it. Figure 1-6(c) shows how AC and DC capability are provided behind every DUT pin using the DIB Access feature.

Multi-Bank Capture Memory

Each instrument has a large block of dynamically assigned capture memory, which varies in depth depending on the particular instrument. The memory is structured such that data from one capture can be moved out concurrently with the capture of data from the next test. Sufficient memory is available for storage of still additional captured data if necessary. This ability to move and capture data concurrently allows for the flexible expansion of both concurrent testing and multi-site parallel test, as needed.

High-speed Back-end Data Move Bus

Each instrument has a high-speed data Move Bus that is used to move captured data off the instrument for processing. Each instrument initiates the movement of the captured data as it completes its measurements, with no test computer intervention. The Move Bus enables movement of data captured in the previous test while the instrument is being set up and data is being captured from the next test. This ability to move and capture data concurrently allows for the flexible expansion of both concurrent testing and multi-site parallel test, as needed.

Multi-Level Signal Processing Architecture

Integra FLEX provides a multi-level signal processing architecture that fully enables concurrent, multi-site testing, *by incurring no parallel test efficiency penalty* as multiple sites are added. This capability is described in the following section.

Multi-Level Signal Processing Architecture

The Integra FLEX signal processing architecture provides a significant improvement in test execution time and enables multi-site, concurrent testing, with no penalty in parallel test efficiency as multiple sites are added. This is achieved by a three-level signal processing architecture that dynamically allocates real-time signal processing power for Background DSP or other processing as instruments and sites are added. Each level is described below.

- Level 1 – Level 1 real-time processing is always available. Complete signal processing is executed in the host test computer.
- Level 2 – Level 2 real-time signal processing is accomplished by the addition of up to eight (8) modular Real-Time Processors to the Integra FLEX system. Once installed, these modules are dynamically brought online as the number of parallel sites increases.
- Level 3 – Level 3 real-time signal processing is available on-board on a per instrument basis.

The assignment of Processor resources among the various levels is handled by the test computer and test program execution environment, with no test engineer intervention. As test data packets become available from the instruments, the Background DSP/Real-Time Processor subsystem dynamically allocates resources as needed across instruments and across sites. If all system DSP resources are busy processing other data, the Background DSP/Real-Time Processor subsystem stores the data in a large memory that is part of the subsystem. Once a DSP resource is available, the data is moved to that resource from processing. In multi-site testing, the system will assign a dedicated Background DSP/Real-Time Processor resource to a particular test site. In this way, as sites are added and DSP resources are licensed to support them, test execution time remains virtually constant. As many as eight (8) auxiliary Background DSP/Real-Time Processor modules can be brought online as the number of parallel sites increases. The system provides sufficient flexibility and horsepower such that throughput only changes by a few percent as additional test sites are added.

Minimization of Shared Resources

One of the more subtle ways that the Integra FLEX supports multi-site, concurrent SOC testing is directly related to the elimination of as many shared resources as possible in the design of the system. By providing certain redundant capabilities on each instrument, the Integra FLEX eliminates the restrictions associated with these capabilities when they are shared within a test system architecture.

As previously described, each Integra FLEX instrument has its own independent clock architecture, Pattern Generator, parameter set memory, PPMU, and can initiate the movement of captured data from its own multi-bank capture memory on its own high-speed Move Bus. In addition, these redundant functional blocks are supported by 1) the ability to control the analog instruments from within the test pattern, 2) the ability to dynamically assign three levels of real-time processing resources wherever they are needed, and 3) the ability to connect any pin to any instrument through the DIB Access feature.

Digital Capabilities for the SOC and DFT Worlds

The Integra FLEX takes the high density CMOS technology of the J750 tester to levels of quality and throughput never before seen for SOC and DFT testing. The Integra FLEX digital instruments provide quadruple the DFT capability of the J750 (4x the scan speed and 4x the scan memory depth), and deliver the preeminent breadth of digital capability at low cost:

- 200 MHz maximum operating speed
- edge placement accuracy to ±250 ps
- 64 Meg vector memory behind each pin
- 48 single-ended pins or 24 differential pin pairs per board
- 1,056 digital pins maximum
- three drivers per pin — large swing, small swing, and 50 Ohm terminated
- 100 MHz MTO with:
  - 24 Meg x 64-bit Captive memory
  - x, y, z address counters
  - algorithmic memory pattern generator
  - software-configurable fail map memory
  - full high-level template support for multiple boards to one site, or multiple sites supported from one board
- 3 Gbits of SCAN data available for every 16 channels that can be configured in any way needed
- SCAN Broadcast capability for parallel test economics and longer equipment lifetime
- Digital Source and Capture (DSSC) provides serial or parallel data at 16 bits wide, with the ability to chain two DSSC blocks together for 32-bit operations
- Six (6) DSSC engines per board
- Fast keep-alive function
- Two high voltage drive pins per board
- DIB Access per four channels/pins
- PMU per pin
- per pin overvoltage/overcurrent protection that disconnects the pin electronics from the DUT on an alarm condition

Resident digital instrument features such as per-pin PMU, fast SCAN, keep-alive, memory test, and flexible configuration, work together to provide the fast throughput needed for the lowest cost digital testing. The Digital Instrument is described in *Section 5, Instrument Description and Specifications*.

Innovative Heritage

The Integra FLEX test system draws on its J750 and Catalyst heritage, and extends their lineage with significant innovation. The Integra FLEX embodies every IP-core Teradyne technology to date and builds upon them to deliver the lowest cost, most flexible, lowest risk DFT to mixed-signal SOC test system available.

Section 2

Meeting Test Floor Objectives

Two of the primary design objectives for the Integra FLEX test system were to 1) enhance manufacturing utilization so that the same test system configurations would be able to accommodate peak levels as well as "normal" levels of demand, so that cost of test would be as low as possible, and 2) increase manufacturing capability so that time-to-volume would decrease, and test system capabilities would always match device test requirements.

Enhanced Manufacturing Utilization

Per Pin Resources

The Integra FLEX instruments are designed to provide a very high level of resources behind each pin:

- per-pin PMU on all instruments
- DIB Access, which allows any pin to be connected to any instrument, without application circuitry
- one or more on-board Time Measurement Units on each DC instrument
- on-board differential voltmeters on each DC instrument
- dual pin high voltage driver on Digital instruments
- 100 MHz self-contained Memory Test and Fail Map Memory on each Digital instrument
- six (6) independent Digital Signal Source/Capture engines each with 128Mbit memory, per Digital instrument
- 3Gbit, totally configurable, SCAN data per 16 channels/pins on Digital instruments
- Keep-Alive function on each Digital instrument
- three LFO/mixers on Microwave instrument suite
- on-board Real-Time processor on Microwave instrument

The feature sets of the Integra FLEX instruments were designed so that, regardless of the instrument configuration on a given test system, the system would have all of the resources needed to fully support the test floor. Even what might be considered a minimal test system configuration, with several each DC and Digital instruments, has the resources for parallel, multi-site tests of continuity and leakage (via PPMUs), and rise/fall times, propagation delay, pulse width, frequency, and period (via TMUs on DC instruments), in addition to DFT techniques and full functional testing. This unprecedented level of high pin functional density offers unmatched utilization with the lowest possible cost system.

Configuration Flexibility

The 24 instrument slots in the Integra FLEX test head accept any instrument. This eliminates a number of constraints and significantly increases flexibility in the placement of instrument types and DIB layout. With the proper planning, instrument configurations and DIB layouts can be created that allow either 1) a single instrument suite to be configured that will test the majority of devices in a product mix, or 2) a multi-site (e.g. quad) test DIB for a single device (e.g. a mixed-signal SOC) can be used on test systems configured not only for that mixed-signal SOC device, but on Integra FLEX test systems configured primarily for linear or digital/SOC devices, with a reduction in the number of sites (i.e. dual versus quad). Figure 2-1 depicts just such a situation. Assume that a device DIB is configured for quad site testing of a mixed-signal device, as depicted in Figure 2-1(a). Some number of Integra FLEX systems on the test floor are configured for mixed-signal, linear/power (Figure 2-1(b)), RF-Microwave (Figure 2-1(c)), and VLSI-Digital (Figure 2-1(d)) devices. A surge in demand occurs for the mixed-signal device; however all of the test systems configured for mixed-signal devices are at maximum capacity.

The red highlighted DIBPogo blocks in Figure 2-1 show the common instrument slot

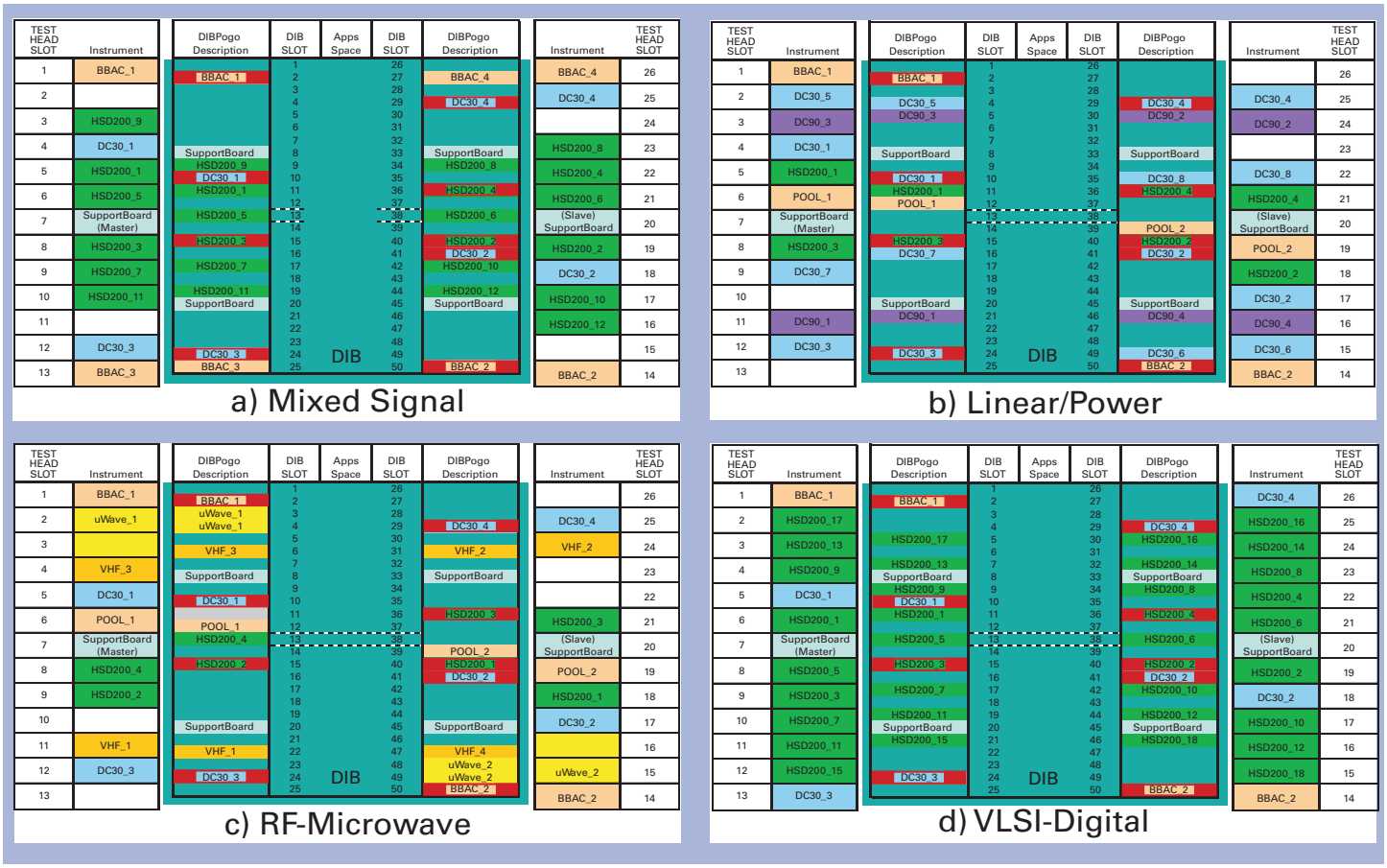


Figure 2-1: Enhanced manufacturing utilization

configurations among the four test system types on the test floor. The mixed-signal DIB can be used directly on any one of the other configured systems to allow testing of the mixed-signal device, at a reduced number of sites. In this way, Integra FLEX can maximize test system utilization, and minimize cost of test.

Performance-On-Demand

The Integra FLEX hardware and software architectures provide for the precise matching of device test requirements and test system capability. In addition to the per pin resources of each instrument and the flexibility of configuring the test head afforded by the universal slot test head architecture, a number of performance features can be enabled (licensed) on-the-fly to precisely match test system capability with device test requirement when and where it is needed. Table 2-1 provides a list of these features and capabilities.

Element	Levels
IX-GL 5.0 Software Tools	
Memory Bitmap	Yes/No (license)
WaferMap	Yes/No (license)
RA+ Redundancy Analysis	Yes/No (license)
Hardware	
Frequency (Mode)	100, 200 MHz
LVM Size	8, 16, 32, 64 M per pin
Memory Test Option (MTO)	0/1 enable
Digital Signal Source/Capture Option (DSSC)	0/1 enable
Gen IV Microwave	0/1 enable
Microwave Splitter	0/1 enable
Phase Noise Option	Yes/No (license)
Microwave Sites Supported	1, 2, 4
BBAC Bandwidth	1 MHz, 3 MHz, 15 MHz
BBAC Source/Digitizer Pairs	1, 2, 4, 6, 8
VHFAC AWG/Digitizers	1, 2, 4, 6, 8
Real-Time Processor Modules	1, 2, 3, 4, 5, 6, 7, 8; added with sites
PicoClock	0/1 enable
DFT Configuration	
Edge Placement Accuracy	±250 ps to ±1 ns
Frequency (Mode)	50 MHz
Edgesets/Timesets	
SVM Usage	

Table 2-1: Performance Licensing

Increasing Manufacturing Capability

The Integra FLEX architecture, instruments, and performance enabling to match device test requirements also contribute directly to increased manufacturing capability. The ability to provide the needed test economics in whatever configuration it is presently in, and minimize the risk associated with expanding to accommodate new devices, allows Integra FLEX to continuously deliver test capabilities matched to the needs of the test floor.

Elimination of Bottlenecks

Manufacturing capability is often significantly impacted by test system architecture issues that can be categorized as "bottlenecks". A brief comparison follows between the Integra FLEX test system and the bottlenecks that typically occur in several key areas of test system architecture.

Non-Pipelined Test Computer/Test System Link

The first is the link between the test system computer and the test system itself. Even using a fiber optic channel at 800 Mbps or more to deliver multiplexed data from multiple test system instruments to the test system computer, the system suffers from the indisputable fact that all of the data has to be concentrated and sent down a single "pipeline". This places constraints on data processing, test setup and execution, and impacts overall throughput. The Integra FLEX test system architecture eliminates the single "pipeline" between the test instruments and the computing resources, by effectively moving the execution of the test program to the instruments, under precise control and coordination of the test system computer. Captured data from any given test need not be sent back to the test computer from the test head for processing, so there is no data concentration to cause a bottleneck. With no data concentration bottleneck, test execution time decreases, with a corresponding increase in throughput.

Background DSP/Real-Time Processing Capability

Even test system computers that have multiple, fast CPUs are limited in how much data can be processed concurrently. This occurs ***after*** the data gets through the link pipeline bottleneck. This problem only increases as more sites are tested in parallel, until throughput is severely impacted, or limits are reached prematurely on the test system's multi-site testing capabilities.

The Integra FLEX test system eliminates bottlenecks due to test program processing requirements, regardless of the number of parallel test sites, with no impact on test system throughput. The Integra FLEX Background DSP/Real-Time Processing capability dynamically assigns dedicated DSP resources to each site as they are needed, or to one or more sites whose processing requirements demand more resources, as appropriate. With three levels of Real-Time Processing available to the data — at the test computer, with the addition of up to eight (8) optional Real-Time Processor modules, and on-board specific instruments — data processing limitations are eliminated, as more parallel test sites are added thereby fully supporting maximum test system throughput.

The Integra FLEX architecture that moves captured data to the Background DSP/Real-Time Processor system from the instruments also contributes significantly to eliminating a major test system bottleneck. Each Integra FLEX instrument has its own dedicated, high-speed data Move Bus to the Background DSP/Real-Time Processing system. Each instrument initiates the movement of data from its capture memory across the Move Bus at the completion of its test routine. Data processing routines for each test are stored in the Background DSP/Real-Time Processing system at test program initiation. As tests are completed and the captured data is received from the instruments, the data is processed immediately. Data processing in the Integra FLEX test system is zero-time processing, further increasing throughput.

Universal Instrument Slots

Many test system architectures require that certain instrument types must reside in specific slots within the test head. This can often place severe constraints on DIB development and overall test system configurations, especially in multi-site applications. This can also impact test system reconfiguration downtime when switching from testing of one device to another. The Integra FLEX test system tester-in-the-test-head architecture provides 24 universal instrument slots, which accept

any Integra FLEX instrument — AC, DC, Microwave, or Digital — for unprecedented flexibility in test head configuration and DIB development, and multi-site test support.

Minimized Shared Test System Resources

The link between the test system and the test computer is the most obvious shared resource within the test system architecture. At any number of places — Pattern Generators (PatGen), data busses, clock subsystems, key functional blocks, and the instruments themselves — shared resources can impose significant constraints at one time or another during test execution. Integra FLEX instruments — AC, DC, Microwave, and Digital — each have their own synchronized DDS clock, PatGen, independent capture data Move Bus, Time Measurement Units (DC instruments), PPMU (AC and Digital instruments), and a number of other functional blocks that in other test systems would be shared resources. This high functional density on each instrument contributes to the lowest possible cost of test delivered by the Integra FLEX test system, makes test development easier, and multi-site test execution more repeatable.

DIB Access

Connecting two instruments such as a V/I and a waveform generator to the same DUT pins on most test systems often requires a significant amount of application circuitry including a number of signal routing relays on the DIB. This increases the complexity of the DIB, provides additional areas where critical test signals can be degraded, and uses valuable DIB real estate best reserved for DUT-specific application circuitry. Integra FLEX eliminates the need for this type of relay circuitry on the DIB because of a feature designed into every instrument referred to as DIB Access. DIB Access provides high performance signal paths that allow a primary and secondary instrument to share access to DUT pins, without the need for relays and applications circuitry on the DIB. DIB Access functionally enables any pin to be connected to any instrument.

Pattern-Controlled Analog Instruments

All Integra FLEX instruments — DC, AC, Microwave, and Digital — have their own independent, on-board clock, Pattern Generator, and parameter set (Pset) memory. Since instrument setups are stored locally in the Pset memory on each instrument, setup commands issued from the test computer can be broadcast to all copies of an instrument so that instrument setup for those instruments occurs simultaneously. Instrument setup instructions can be embedded in the test pattern, so as the pattern is executed on each analog instrument, those setup instructions are executed directly by the instrument, under precise timing control of the pattern. This ability significantly improves test repeatability, due to the precise timing control of the instruments from the pattern and their synchronization. Test execution time is reduced as well, since instrument setup commands execute locally from Pset memory, and need not be transmitted from the test computer each time they are required.

Each instrument initiates the movement of its captured data from its capture memory over its dedicated Move Bus to the Background DSP/Real-Time Processor system for processing. While the data from a previous test is being moved, the instrument can be setup and begin capture for the next test. This ability also reduces test execution time.

Section 3

Improving Time-To-Market

Integra FLEX provides both software and hardware vehicles that significantly improve time-to-market by leveraging prior investments on the production floor. The test development and execution environment plays a critical role in that leveraging ability, and is discussed here within that context. Please refer to *Section 4, Multi-Level Test Development: IG-XL 5.0* for more detailed information.

Unrestricted Test Development

Complex devices require complex test programs. Test systems that don't leverage the expertise of more experienced test engineers for use by less experienced ones, create a bottleneck in the test development effort, and waste prior expenditures in development time and effort. Test development environments that do not provide both intuitive graphical test development tools as well as code-based tools, create a test development bottleneck by forcing every test engineer, regardless of experience level, to learn the test system coding language. This places significant constraints on less-experience test engineers who need to make as important a contribution to time-to-market and time-to-volume as their more experienced colleagues. The Integra FLEX IG-XL 5.0 test development and execution environment eliminates these barriers by providing a hierarchy of test development tools that range from simple, graphically-based templates, to extremely powerful code-based program development. Integra FLEX test programs are fully supported by the concept of "develop once and reuse often". Test templates, elements, and procedures developed by one test engineer can be fully documented using integral HTML Help documentation generation tools so that another engineer can quickly understand how to use them for their own development efforts. Test templates, elements, and procedures developed by test engineering are appended to the extensive library of pre-developed and proven test procedures supplied with the Integra FLEX test system. In this way, prior test development effort is fully leveraged for the program under development.

Precision Synchronized Cross-Domain Debugging

Devices with disparate functional blocks require concurrent testing in order to guaranteed device performance and freedom from interaction among those functional blocks. If the test system cannot fully "line up" all digital and analog events at the precise time of a test failure, the test engineer is virtually guaranteed extended test debug time and effort. The inability of a test system to adequately provide completely synchronized event information, across all instrument types — AC, DC, Microwave, and Digital — at any point in the execution of a test program, can be a significant bottleneck in test development and debug. Integra FLEX overcomes this test debug bottleneck because of the Integra FLEX TimeTrack™ system. TimeTrack is the combination of the per instrument architectural elements (i.e. clock, PatGen, Pset memory, etc.) and the debugging tools within the IG-XL 5.0 test development environment, which when taken together provide this capability. The TimeTrack precision phase alignment capability is built-in to the Integra FLEX instruments, and enabled by the TimeTrack tools supplied as part of the Integra FLEX IG-XL 5.0 test development and execution environment. TimeTrack enables all Integra FLEX instruments — AC, DC, Microwave, and Digital — to respond to Halt-On-Failure signals from any other instrument, and for the debug software to "know" their precise position in their respective test patterns, so that every event at the precise point of failure can be "lined up", and analyzed, in context, as quickly as possible.

Integrated Tools

Integra FLEX and IG-XL 5.0 provide a suite of integrated tools to support design-to-test pattern translation, test simulation, and DFT. For a detailed list of Teradyne's working partners in design-to-manufacturing solutions, please refer to *Section 4, Multi-Level Test Development: IG-XL 5.0*.

Simplified Docking and Production Integration

A significant amount of effort has gone in to the physical design of the Integra FLEX so that the investments made in proven solutions for previous platforms are completely leveraged for use with Integra FLEX. Special effort relative to mechanical docking issues and interfaces for probers and handlers allow Integra FLEX to fully leverage these time and resource-intensive expenditures in order to minimize their impact on time-to-market.

Table 3-1 lists the probers and handlers for which Integra FLEX interface solutions are currently available.

Integra FLEX/Catalyst Prober Interface Configurability

Integra FLEX prober interfaces are configurable with Catalyst prober interfaces. The Catalyst L-Plate is removed and permanently replaced with a no-charge Integra FLEX/Catalyst compatible L-Plate. Two course alignment pins, three Kinematic dock grooves, and three groove spacers are removed from the Catalyst L-Plate and reused on the Integra FLEX L-Plate. Five additional parts are required to complete the Integra FLEX/Catalyst Prober Interface upgrade. After the upgrade, moving between the Catalyst and Integra FLEX involves an exchange of the Tower/Flange assembly, and the removal or addition of a Quick DIB Clamp Plate (QDC) as required.

Integra FLEX/Catalyst Handler Interface Configurability

Integra FLEX handler interfaces are configurable with Catalyst handler interfaces. The Catalyst Handler plate, insert, and three groove spacers are removed and permanently replaced with a no-charge Integra FLEX/Catalyst compatible Handler plate, insert, and v-grooves. Four additional parts are required to complete the Integra FLEX/Catalyst Handler Interface upgrade. After the upgrade, moving between the Catalyst and Integra FLEX involves an exchange of the HIB insert, and the removal or addition of a Quick DIB Clamp Plate (QDC) as required.

Integra FLEX/J750 Interface Configurability

Integra FLEX interfaces are planned to be configurable with J750 interfaces. Please refer to separate product roadmap documents for a schedule of availability.

Handler/Prober Communications

GPIB drivers exist for most handlers and probers. The serial driver supports IEEE-P849 protocol, while the parallel TTL driver supports 32, 64, or 96 I/O ports. GPIB interfaces can be mounted in the Auxiliary Equipment Cabinet. KLA Integrator support is included, which allows job load and data collection using the Prober control panel.

Available Interface Solutions
Probers
EG 40XX Top and Bottom Load
EG 5300 Top and Bottom Load
TEL P8XL Top and Bottom Load
TEL P12XL Top and Bottom Load
TSK UF200 AL Top Load
TSK UF200 FL Bottom Load
TSK UF200S Bottom Load
TSK UF200/APM 90 Top and Bottom Load
TSK UF300 Top and Bottom Load
Handlers
DeltaFLEX
Delta Castle
Seiko-Epson NS5000/NS6000
Synax 1701
Synax 1121

Table 3-1: Integra FLEX interface

Section 4

Multi-Level Test Development: IG-XL 5.0

Key Objectives

From the onset, it was clear that the test development environment necessary to support the flexibility and breadth of application of the Integra FLEX test system must itself be highly flexible and address a breadth of concerns and issues spanning diverse environments:

- Test/Product Engineer Background
  - Senior versus junior
  - Digital versus mixed-signal
  - Specific device applications
  - Specific test platform
  - Business Model
  - Integrated Device Manufacturer (IDM)
  - Fabless
  - Contract manufacturer/test house
- Available Resources
  - Test program converted from similar test platform versus different platform
  - Test program converted with test waveforms, procedures, DSP algorithms, etc. available
  - New design, platform, and application
- Design and Process
  - Design well known, already in production versus new design
  - Design is merge of IP cores from various design companies (IDM, fabless, etc.)
  - Well-controlled process versus new process

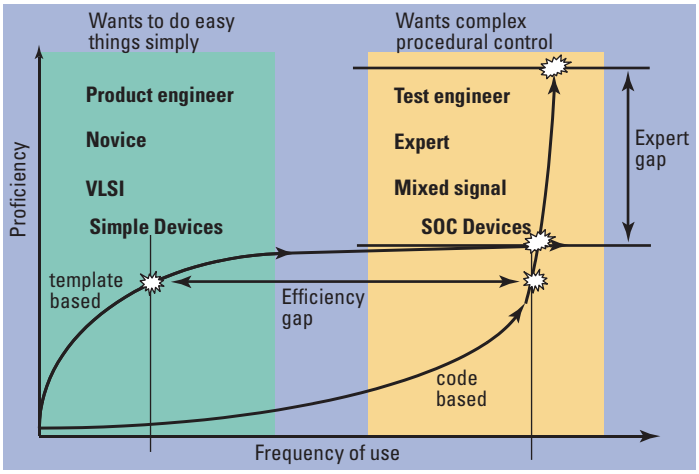


Figure 4-1: Diversity of test environments

From these concerns and issues, three prime objectives were identified that the Integra FLEX test development environment must meet:

- Extend the J750 IG-XL software to provide a common platform for the entire Integra family of general-purpose testers
- Provide a multi-level programming capability to accommodate a diverse development environment, and enable a shorter development time
- Provide an advanced linear and mixed-signal use model and toolset to build on the DUT-centric test development environment of IG-XL

The result of achieving these three objectives is the device-oriented programming and debug environment embodied by Integra FLEX IG-XL 5.0.

Multi-level Programming Capability

Integra FLEX IG-XL 5.0 is built upon the foundations of Teradyne J750 IG-XL, which carries forward key concepts from IMAGE, and represents a community of several thousand users, and a combined development effort of over 730 person-years of engineering. From that experience base, Integra FLEX IG-XL 5.0 provides a test development environment that allows both highly experienced and novice programmers alike to rapidly develop fully functional test programs from an intuitive, graphical user interface, based on the Microsoft Excel® spreadsheet paradigm. In its simplest form, device specifications, timing, levels, and edges are entered into pre-formatted test templates, and the fully functional test program is generated from the filled in templates. In a manner of minutes, a novice can have a verified test program ready to run, without learning any of the Integra FLEX programming language. Refer to Figure 4-2. At its most complex, an experienced programmer can re-use previously developed test templates and elements, flow them together to create a procedure, write code-

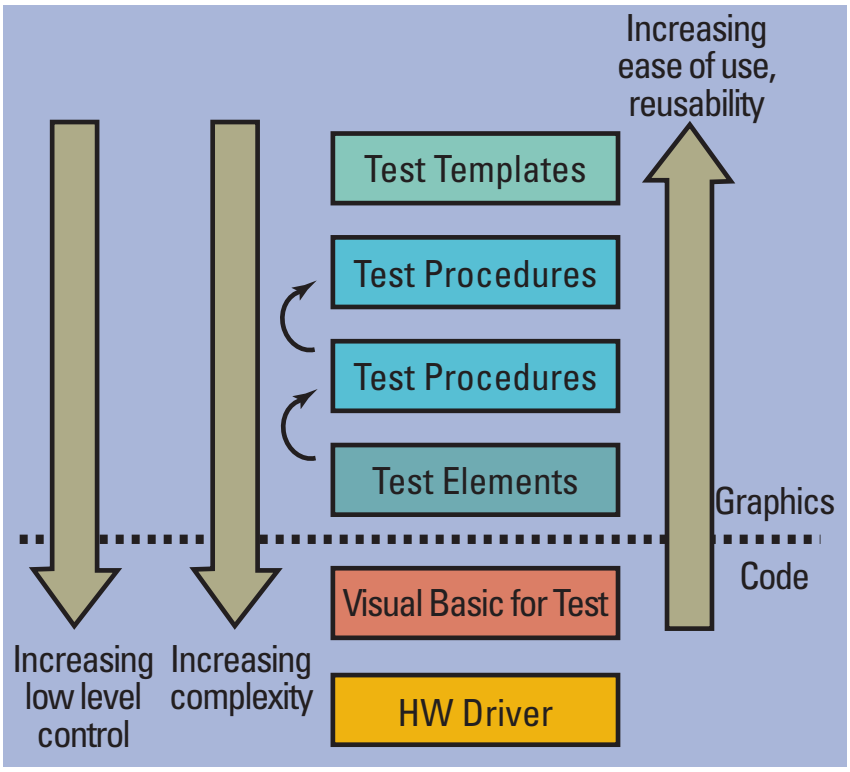


Figure 4-2: Programming levels

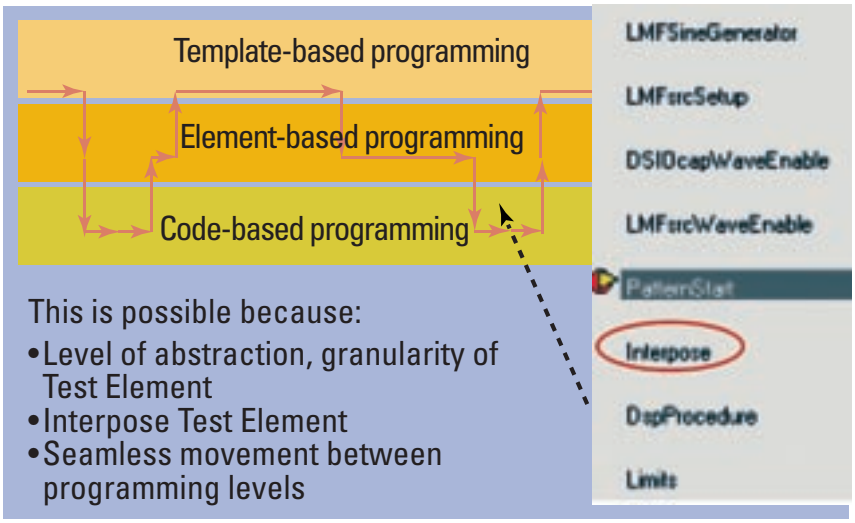
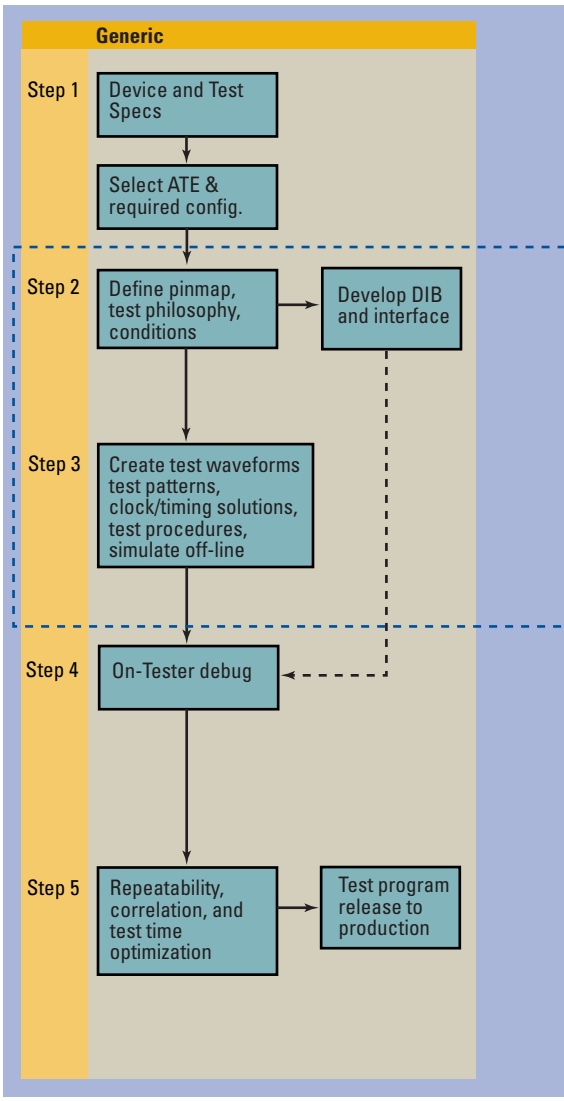


Figure 4-3: Seamless integration of programming levels



based routines that are then selected from template pull-down menus to become part of that procedure (or any other), to create a test program for a mixed-signal SOC device. IG-XL 5.0 provides an environment where all test development can remain within the graphical user interface, unless custom device issues or the augmentation of test functionality require code-based development. Refer to Figure 4-3.

The general approach to programming within the IG-XL 5.0 environment is the entry of device data in an enhanced spreadsheet. The flexibility of IG-XL 5.0 allows both fixed numbers as well as equations with variables to be entered into device parameters, allowing the rapid development of relational test parameters such as might be used for range or limit testing. Device pin names and timing relationships are entered into the spreadsheet, and the software determines how best to configure the instruments to support that timing relationship, within the capabilities of the test system. Should a set of device parameters or timing relationship be defined that cannot be

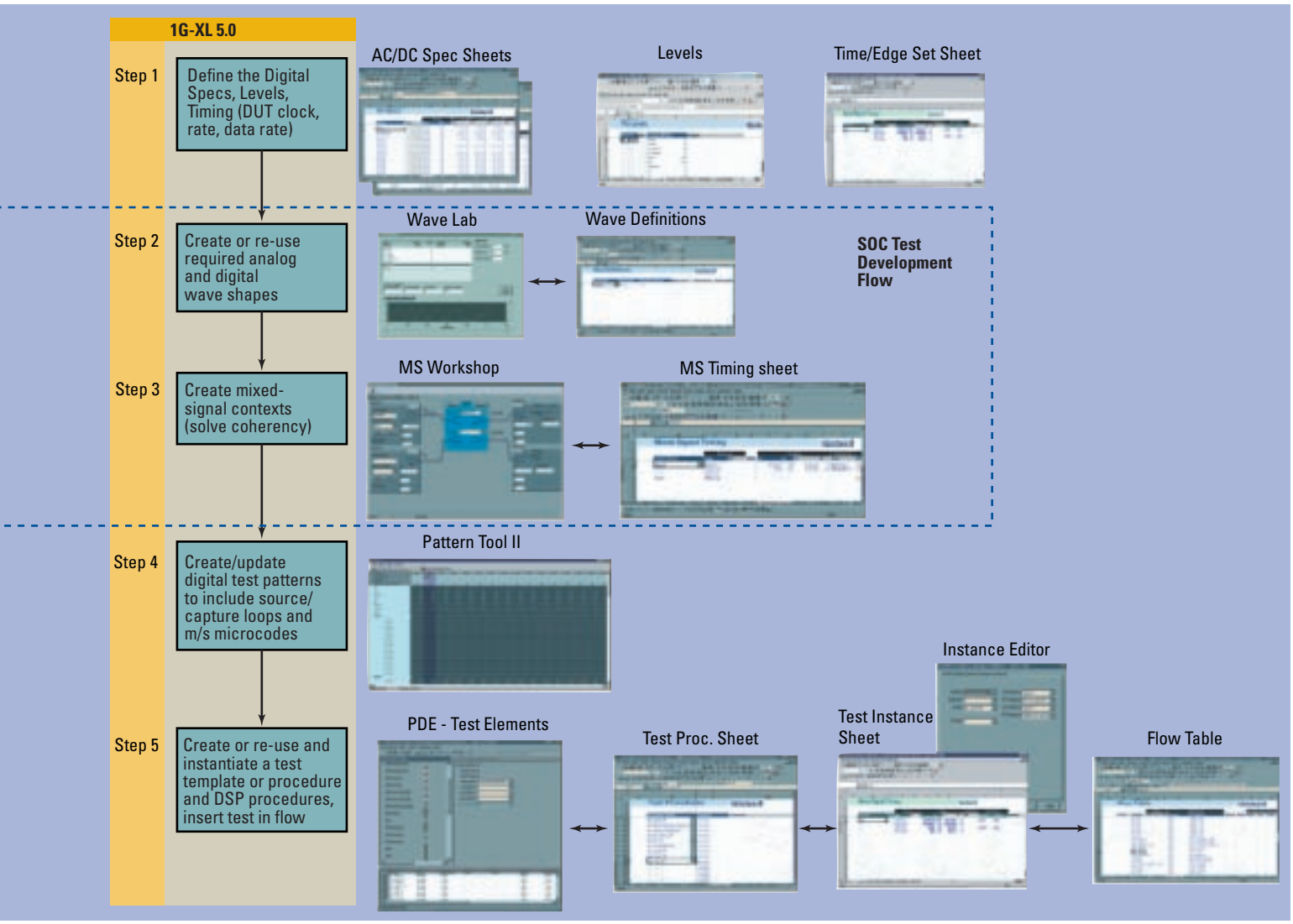


Figure 4-4: Generic vs. IG-XL 5.0 test development flow

supported by the test system with full accuracy and performance, the programmer receives immediate feedback, so that any required adjustments can be made. In this way, the programmer need only think about the device under test, and not the test system.

As experienced programmers code and build custom, complex, template-based test elements, routines, and procedures, they have the tools available to automatically generate HTML help documentation, with tool tips, to guide less experienced programmers in their setup and use. This system-generated help documentation, along with library functions, is one of the features of IG-XL 5.0 that enables a "design once, re-use many times" approach to the test program development process.

Recognizing that programmers may come to the Integra FLEX IG-XL 5.0 environment with a variety of platform experience, IG-XL 5.0 features a standardized, familiar interface that is consistent with industry practice.

Device-centric Test Development

General DataTool™ Overview

Figure 4-4 illustrates the difference in the overall test development flow between a tester-centric approach and the Integra FLEX device-centric approach, and provides a glimpse of the tools available to enable that development to occur in the shortest possible time. As is readily apparent, each of the steps and the tools used to support them all define their required data in terms of device specifications and parameters. Existing test elements and procedures are re-used either as is, or

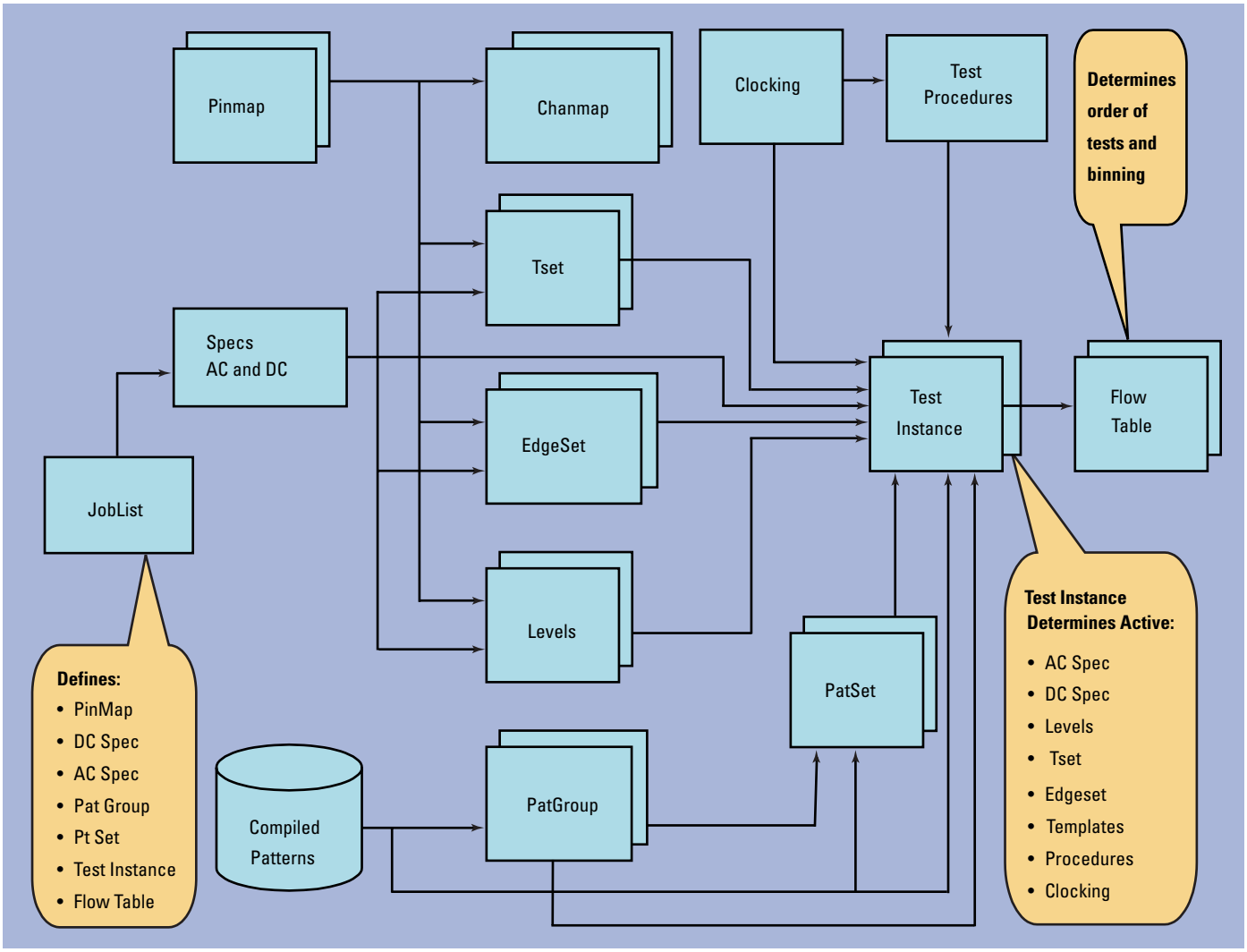


Figure 4-5: IG-XL 5.0 workbook architecture

instances of those elements and procedures are quickly and simply created to satisfy the specific device requirements.

The device data is organized into the following general categories:

- Pinmap
- Tester Channel Map
- Device Specs (AC & DC)
- Timing and Formatting (based on device specs)
- DC and Pin Levels (based on device specs)
- Test Instances (based on templates and procedures)
- Mixed-Signal Test Waveforms and Setups
- Digital and Mixed-Signal Patterns
- Program Flow and Binning

Figure 4-5 depicts the overall test flow block diagram, and how the various device data and their respective spreadsheet tools within the DataTool environment interrelate. Each is briefly described below. Those spreadsheets and tools specific to digital and mixed-signal development are described in the following sections. The descriptions below assume that the test program is being built and debugged for a single (first) site (Site 0). Multi-site capability is added by duplicating worksheet columns for N additional sites. All tools and templates adapt automatically to multiple sites. Please refer to the later section ***Native Multisite Capabilities*** for more information on IG-XL V5.0 multi-site capabilities.

Pin Map

The Pin Map Sheet (refer to Figure 4-6) provides a worksheet for entering the names of the device pins as they are defined on the device pin-out diagram. A pop-up menu allows rapid definition of the type of pin, (i.e. I/O, input, output, analog, power, etc.). Comments regarding the pin function are entered as well. The Pin Map defines the interface to the device, in device terms.

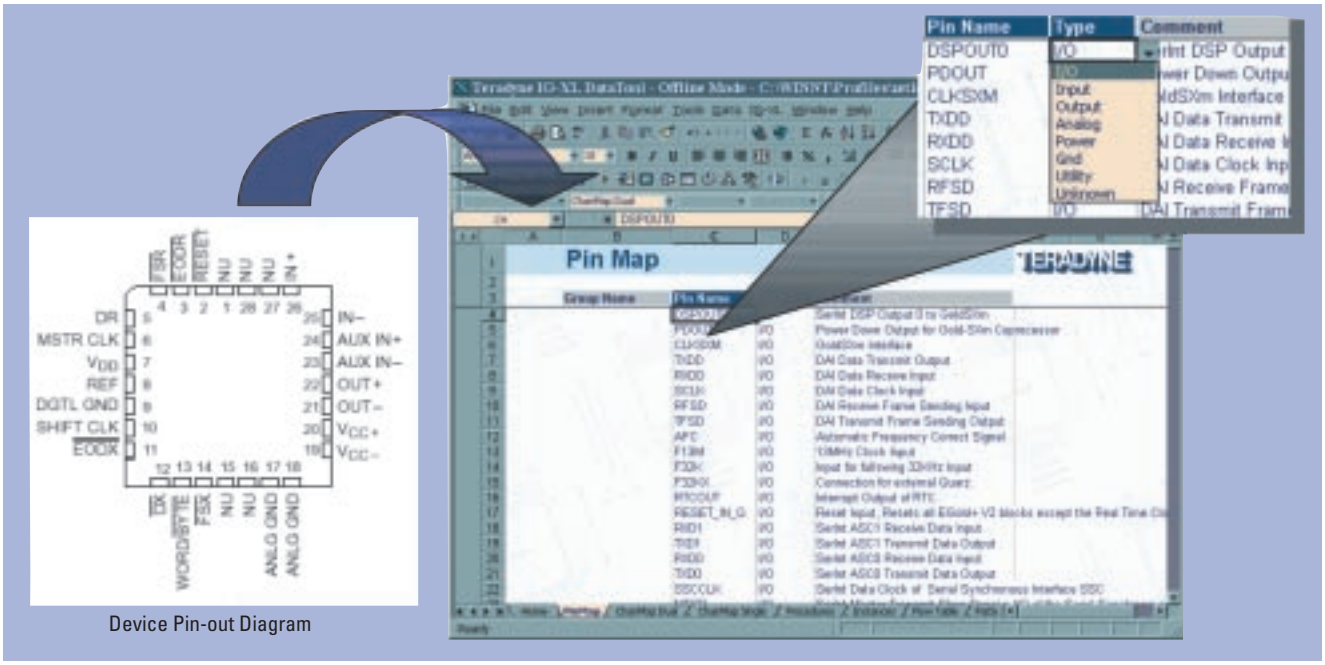


Figure 4-6: Pin map worksheet

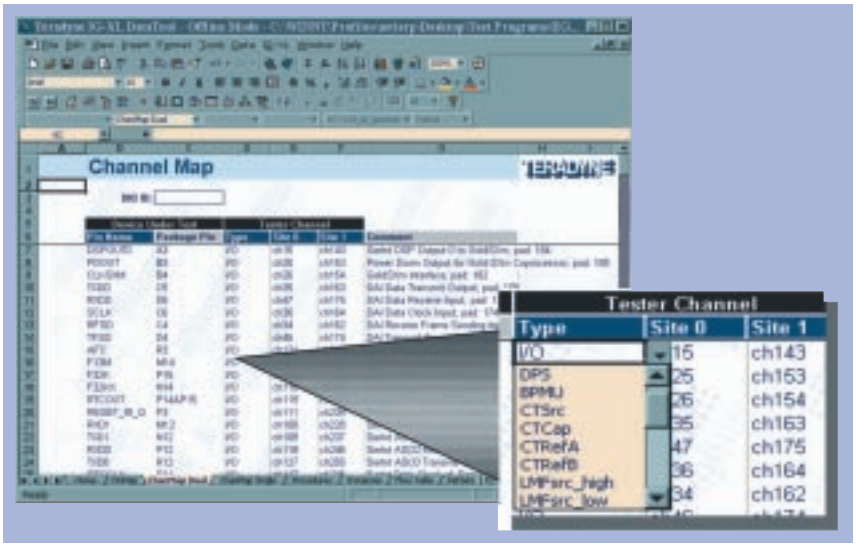


Figure 4-7: Channel map worksheet

Channel Map

The data defined for the device in the Pin Map is automatically made available in the Channel Map worksheet, where the specific pins of the device under test are assigned to the hardware channels of the test system for Site 0. Pop-up menus allow rapid assignment of tester resources to each device pin, and the menus are "smart", in that they only display those tester resources appropriate for that given pin type. Refer to Figure 4-7.

Device Spec Sheet

The device specifications are entered into the Device Spec worksheet directly from the device Specification or Data Sheet. Spec qualifiers (i.e. minimum, typical, or maximum) are selected from pop-up menus allowing rapid data entry. Refer to Figure 4-8.

Timing and Format Setup

Device timing and format information are entered into the Timing Sets worksheet directly from the interface specifications. Refer to Figure 4-9.

DC and Pin Levels

DC parameters and pin levels are entered directly from the device specification or data sheet into the DC Spec worksheet. Refer to Figure 4-10.

PDE-Procedure Development Environment

The Procedure Development Environment (PDE) (refer to Figure 4-11) provides a centralized, coordinated display for all facets of test procedure development. The PDE provides a graphical representation of the test procedure flow, with test elements identified by name and iconic representation. An Element Editor allows arguments to be defined for each test element. A Variable Table area provides a table for the input of parameters and where the setup of conditions for inter-element communications occur. An Element Chooser provides a simple means to select various test elements by name, category, or instrument. The Test Instance Editor can be invoked for creating customized test templates. The Instance Editor Wizard generates test instances quickly and reliably through a simple difference selection process.

Test Instances – Design Once, Re-use Many Times

IG-XL V5.0 provides the Test Instance Editor which allows a test procedure to be written once, and easily adapted to "flavors" of a device. Perhaps the device is offered in several package configurations, or different performance "grades". Both instances are easily accommodated. As described above, the specifications for each "instance" of the device are entered into the appropriate worksheets. At test load time, the specific Pin Map, Timing, or Device Spec sheet is selected, and the test procedure is compiled to match that specific "flavor" of the device. Characterization can be performed on any test instance with no special template required. Refer to Figure 4-12.

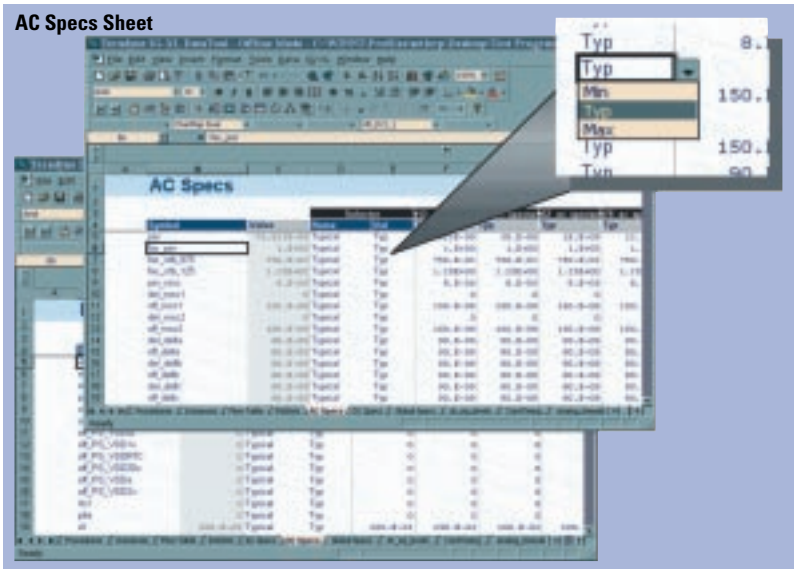
Standard Test Templates

Integra FLEX is supplied with a library of pre-built templates for a variety of tests that are common to all devices. This existing library of templates allows programmers to concentrate their efforts on device-specific test development. Templates are supplied for digital functional tests (patterns), continuity, power supply devices, and parametric tests. Device-specific data need only be entered into the templates to generate those tests. The tests these templates generate are extensible through custom templates if required. The specific test templates provided are:

- Functional (BIST, SCAN)
- Pin PMU/Board PMU (DC parametrics)
- Power Supply (ICC, Iddq)
- A/D and D/A Converter
  - Differential Linearity Error
  - Integral Linearity Error
  - Offset Error
  - Absolute Error
- MTO Embedded Memory

Test Debug Environment

The Test Debug Environment (TDE) is fully integrated with the PDE within IG-XL V5.0. Refer to Figure 4-14. The procedure can be stepped through, while trap points and test flow are displayed. All tools are in one frame. Preferences for each tool can be set. The tools used in the last debug session are remembered and opened automatically to where the session was saved, with all tools synchronized. Through the Instrument Debug Display, read-write access to tester instrument states is provided, allowing



Symbol	Parameter	Test Conditions	Min	Max	Typ	Unit
V_{CC}	Power		4.5	5.5	5	V
V_{IL}	Input Low Level		-0.5	0.8	0	V
V_{IH}	Input High Level		0.7 V_{CC}	V_{CC}+0.5	5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, V_{CC} = V_{CC} min		0.45	0.8	V
V_{PPL}	V_{PP} During Read-Only Operations	Note: Erase/Programs are inhibited when V_{PP} = V_{PPL}	0.00	6.5	5	V
V_{PPH}	V_{PP} During Read/Write Operation		11.40	12.60	12.6	V

Figure 4-8: Device spec worksheet

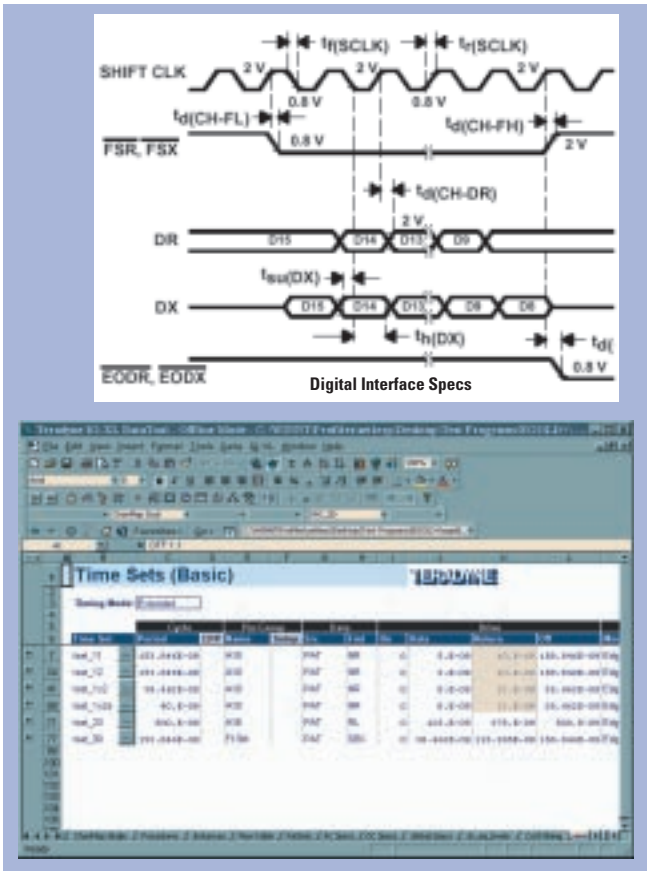


Figure 4-9: Timing sets worksheet

Symbol	Parameter	Test Conditions	Min	Max	Typ	Unit
V_{CC}	Power		4.5	5.5	5	V
V_{IL}	Input Low Level		-0.5	0.8	0	V
V_{IH}	Input High Level		0.7 V_{CC}	V_{CC}+0.5	5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, V_{CC} = V_{CC} min		0.45	0.8	V
V_{PPL}	V_{PP} During Read-Only Operations	Note: Erase/Programs are inhibited when V_{PP} = V_{PPL}	0.00	6.5	5	V
V_{PPH}	V_{PP} During Read Oper		11.40	12.60	12.6	V

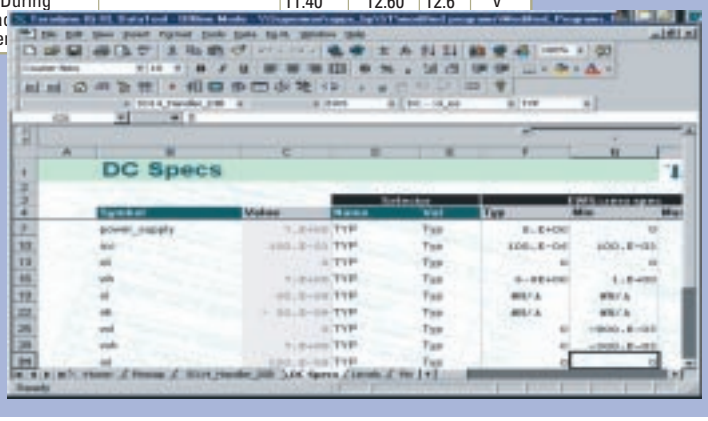


Figure 4-10: DC spec worksheet

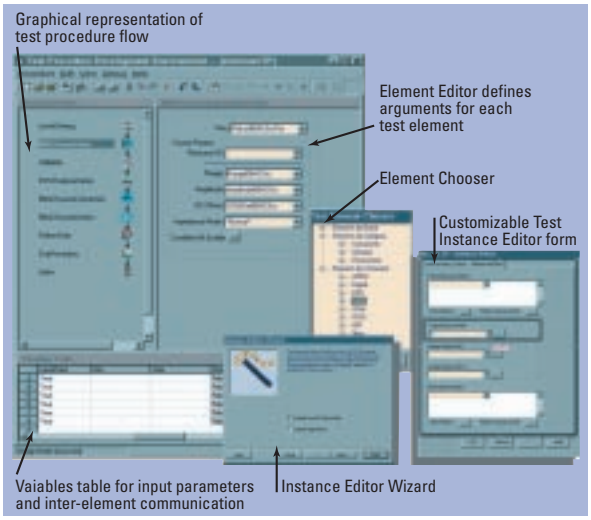


Figure 4-11: Procedure development environment

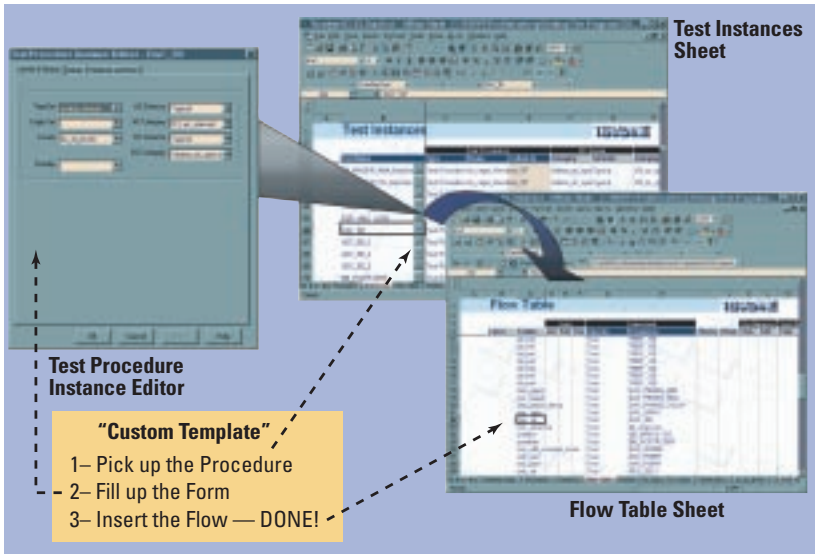


Figure 4-12: Test instance editor

program debug at the tester hardware level, when needed.

Several of the specific tools for both digital and mixed-signal SOC debug are described below.

Digital

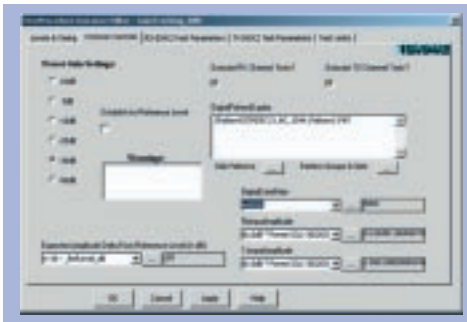
Test development and debug for digital devices is approached in the same manner and using all of the worksheets as described above. IG-XL V5.0 is equipped with a fully integrated suite of tools specifically designed to bring the power of IG-XL V5.0 to digital test development and debug.

Pattern Tool II

Pattern Tool II provides a highly integrated suite of tools for working in the digital domain. Within the tool, vectors and patterns may be loaded, reviewed, edited, run, and verified. The microcode that controls analog and DSSC instruments can be reviewed and edited. Psets, which define instrument setups from within the pattern for mixed-signal SOC testing, can be defined and edited as needed. Patterns may be searched for failures. A long list of development functions can be accessed from the central, coordinated environment of the Pattern Tool. Refer to Figure 4-16. The Pattern Tool II provides the ability to precisely "line up" all test events to debug a test failure across multiple domains (i.e. analog and digital).

Test Instance Editor

Figure 4-17 illustrates the case of the Test Instance Editor being used for a digital device. The same philosophy of design once, re-use many times applies to digital patterns and test procedures.



- Initial form automatically created by PDE Wizard
- Layout/contents can be improved in Visual Basic development environment
- Functionality is similar to Test Templates, but allows creation of more complex test functions

Figure 4-13: Instance editor customization

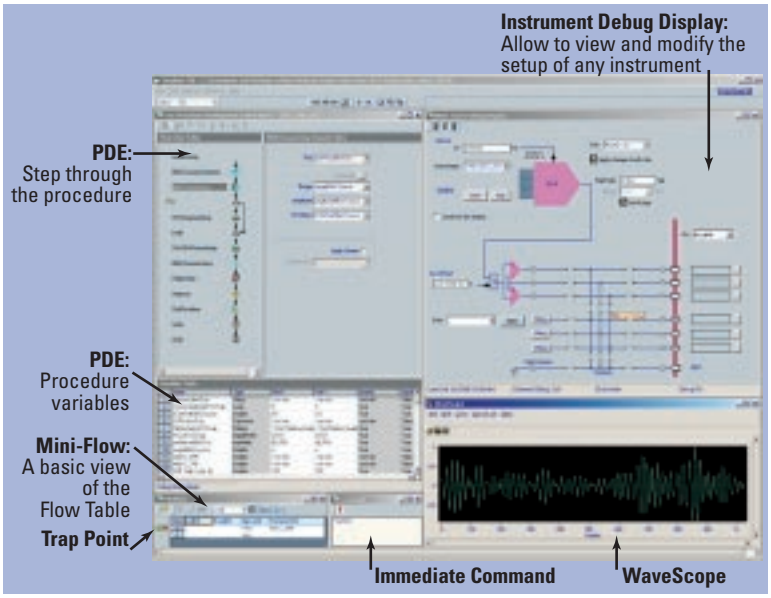


Figure 4-14: Test debug environment

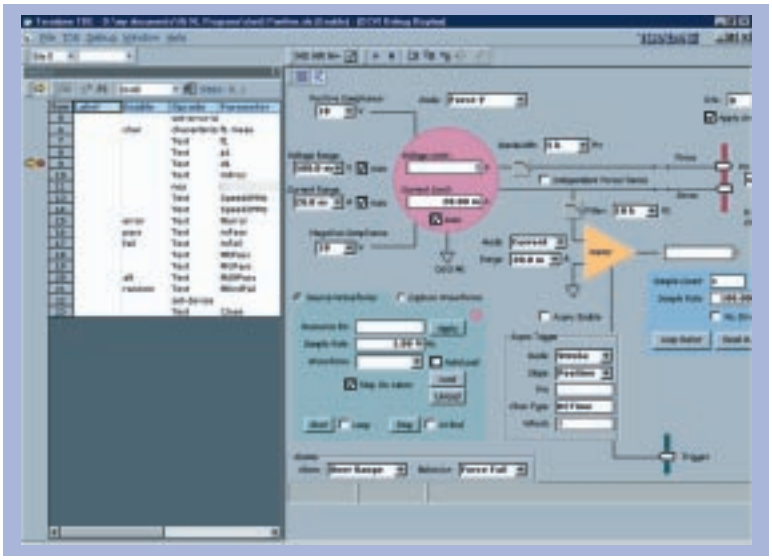


Figure 4-15: Hardware-level debug

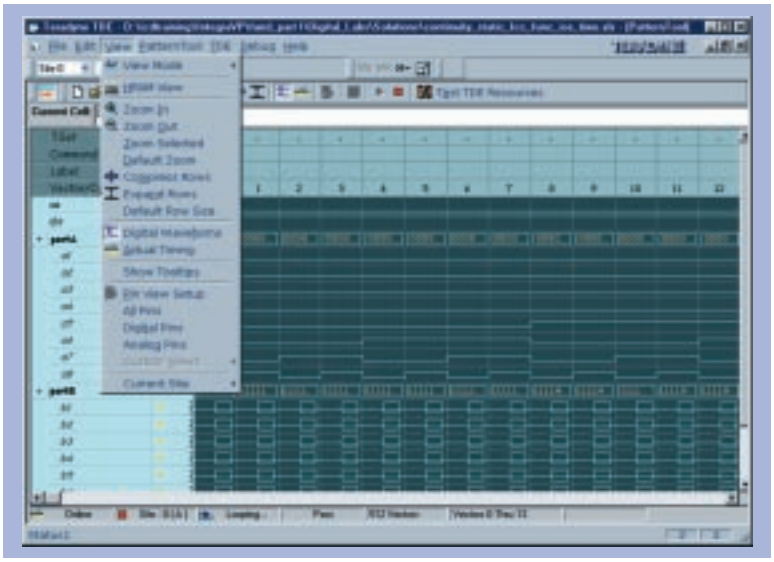


Figure 4-16: Pattern Tool II main screen

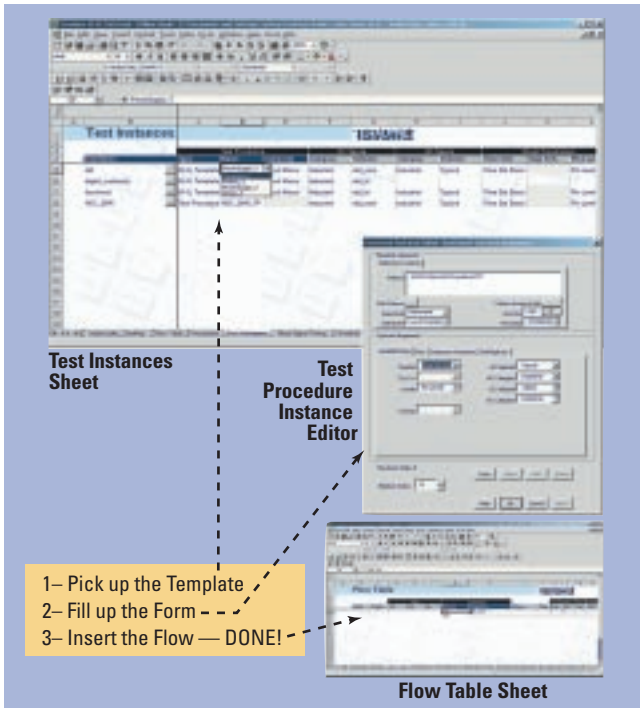


Figure 4-17: Fast test development through template re-use

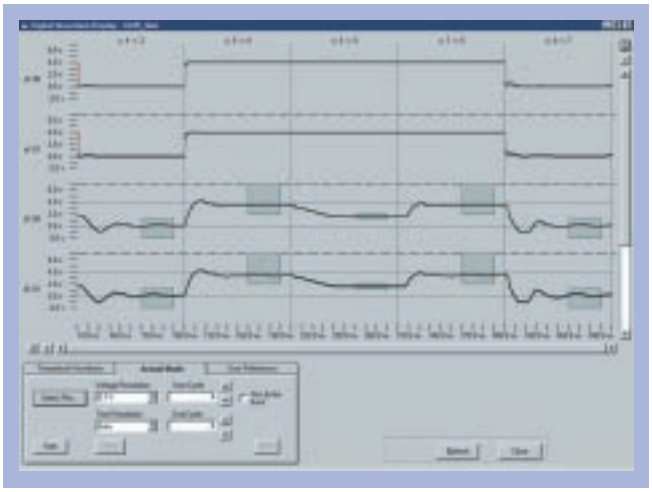


Figure 4-18: Digital waveform display

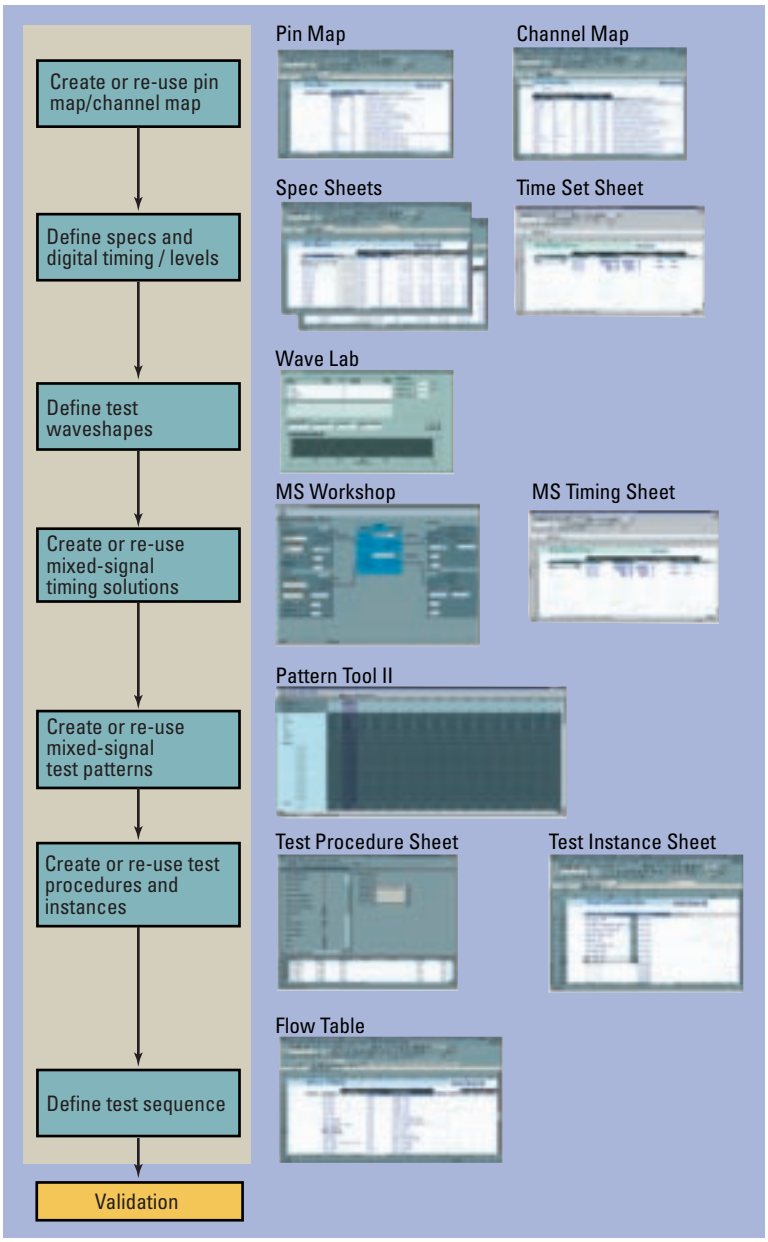


Figure 4-19: Mixed-signal test development flow

Digital Waveform Display

Figure 4-18 is a screenshot from the Digital Waveform Display. Based on the entries made in the timing and level worksheets, a graphical representation of how the timing sets are defined is displayed in the Digital Waveform Display.

Mixed-Signal SOC

Test development and debug for mixed-signal SOC devices is approached in the same manner and using all of the worksheets as described above. IG-XL V5.0 is equipped with a fully integrated suite of tools specifically designed to bring the power of IG-XL V5.0 to mixed-signal SOC test development and debug.

Test Development Flow

Figure 4-19 illustrates the test development flow for mixed-signal devices. The process is essentially the same as described earlier in the general case; however, IG-XL V5.0 provides an integrated tool suite specifically tailored to the tasks of mixed-signal device test programming.

WaveDesigner

The WaveDesigner tool provides a graphical workspace where complex waveforms can be defined quickly and easily from simpler shapes and basic functions. A vertically-sliced, extensible library of basic and complex functions allows pull-down menu selection of waveform components. Relative frequency and amplitude parameters allow simple re-use of the waveform.

WaveScope

The WaveScope tool provides a graphical display of waveform data. It supports the display of waveforms created in the Mixed-Signal Workshop (MSW), text files, and IMAGE .WAV files.

Mixed-Signal Workshop (MSW)

The Mixed-Signal Workshop (MSW) provides a graphical environment with the required tools to resolve complex mixed-signal timing requirements. The timing solution generated by the MSW takes into account the specifications of the DUT, the capabilities of the test system instruments, and the specific test conditions defined in the MSW. All instruments used in a given test are integrated into the MSW environment. When the MSW responds with a listing of timing solutions alternatives, the programmer can see at a glance what test constraints there may be, and how they will affect the test results. The timing solution is generated by the MSW, based on the requirements of the DUT, with no intervention by the programmer.

Putting it All Together

Figure 4-24 illustrates how each of the available tools interrelate, and how the modular object-oriented programming environment allows the re-use of mixed-signal test building blocks such as test waveforms, coherent timing solutions, and DSP routines.

Background DSP Environment

Figure 4-25 illustrates how the Background DSP functions relate to a sample test program.

A Pset embedded in the test pattern sets up an analog digitizer instrument for each of four sites simultaneously. The capture of the waveform is initiated and the data is captured to memory. Upon completion of the capture, each instrument initiates the movement of the captured data to the Background DSP subsystem, with no tester computer intervention. The DSP procedure associated with the particular test is started automatically, again with no tester computer intervention.

The architecture of the Integra FLEX and IG-XL V5.0 provides a distributed DSP solution that scales completely with additional test sites.

Native Multi-site Capabilities

The two primary issues which must be addressed by the test system relative to parallel test are multi-site support and efficiency. How well the tester supports the transition from single site, to dual, to quad, to octal site, and beyond, plays a critical role in both time-to-volume and time-to-market. Multi-site test capability should fully support maximum system throughput, with a minimum development effort.

IG-XL V5.0 and the Integra FLEX hardware assume multi-site testing, and in fact, to the IG-XL V5.0 environment, single site testing is an anomaly, useful only for debugging a test program. A valid test program generated by IG-XL V5.0 for a single (first) site (Site 0) is site-neutral. Adding additional sites only requires changing the Channel Map, which is done by duplicating the Tester Channel column for the number of sites required, and assigning instrument resources to the correct channels. Refer to Figure 4-27. The test program will recompile for a multi-site test program, with all tools instantly updated to reflect the additional sites. Once a multi-site test program is built, any changes to Site 0 are replicated through to the other sites automatically. This translates to a 90-99% multi-site efficiency.

IG-XL V5.0 and Integra FLEX provide built-in support for up to 32-site parallel test (IG-XL V5.0 supports custom solutions with up to 128 sites), with 90%+ efficiency. Refer to Figure 4-28. With the Integra FLEX test system, increasing the number of sites tested in parallel ***does*** increase throughput per tester. The autonomous nature of the instruments and the elimination of test system bottlenecks enable the increase in

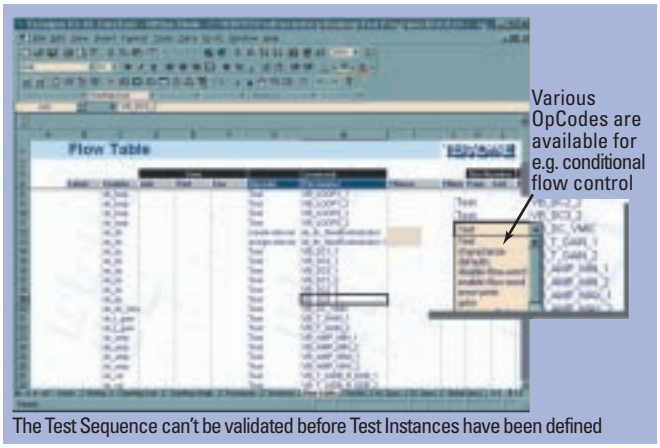


Figure 4-21: Mixed-signal test sequence definition

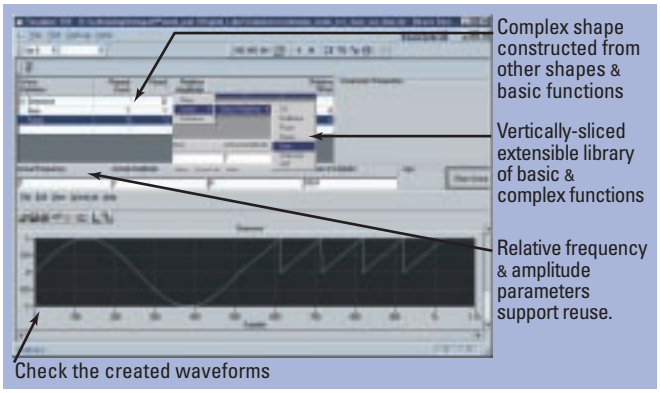


Figure 4-22: WaveDesigner tool

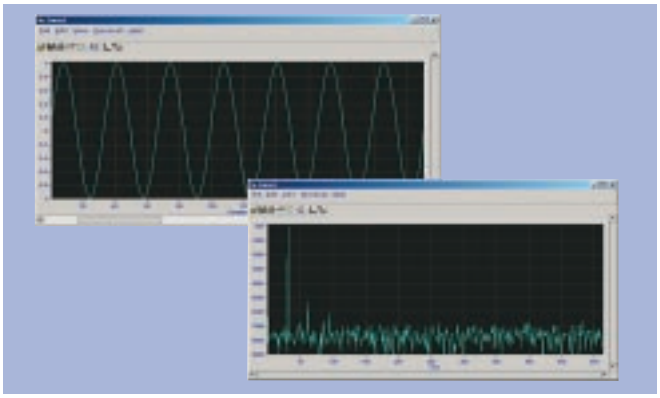


Figure 4-23: WaveScope tool

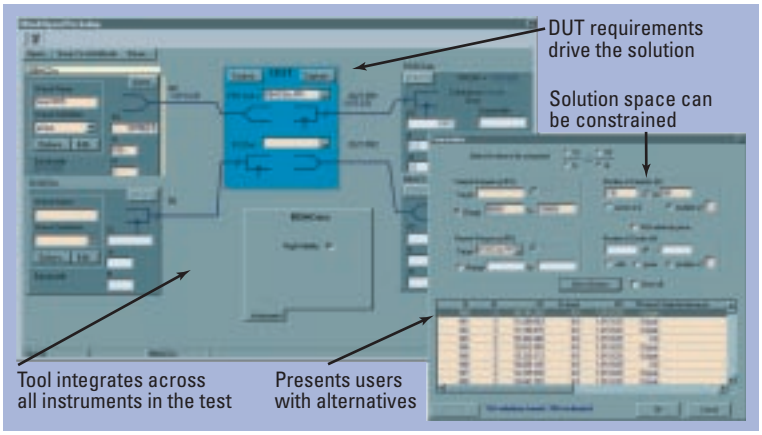


Figure 4-24: Mixed-signal workshop

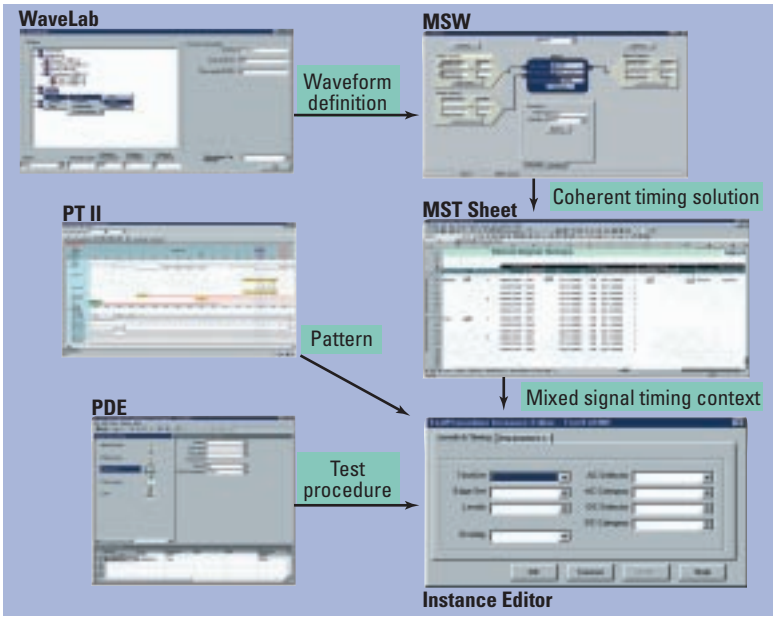
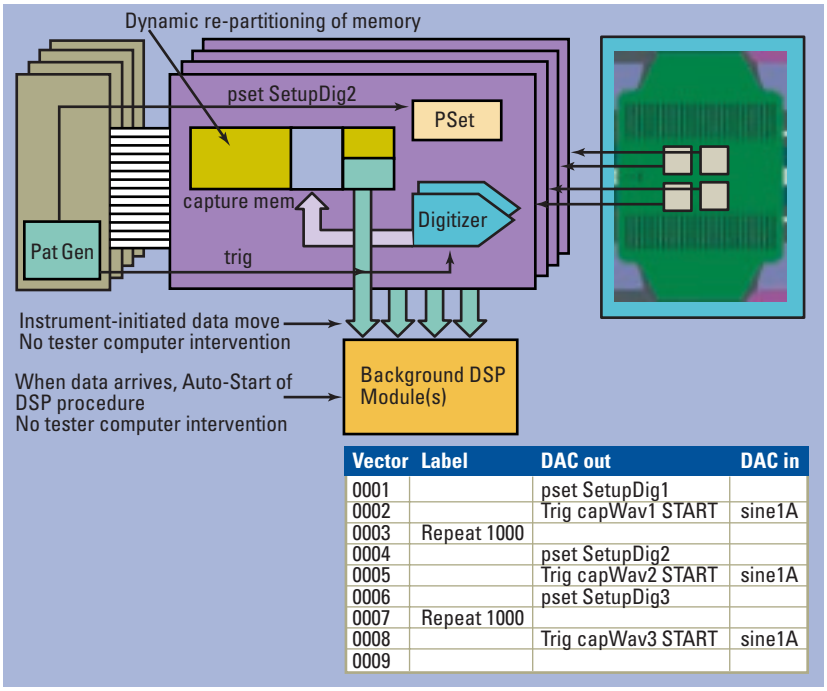


Figure 4-25: Mixed-signal re-usable components overview



Vector	Label	DAC out	DAC in
0001		pset SetupDig1	
0002		Trig capWav1 START	sine1A
0003	Repeat 1000		
0004		pset SetupDig2	
0005		Trig capWav2 START	sine1A
0006		pset SetupDig3	
0007	Repeat 1000		
0008		Trig capWav3 START	sine1A
0009			

Figure 4-26: DSP development procedure

throughput as the number of sites increase. The modular approach and dynamic assignment of DSP resources also enables the increase in throughput as the number of sites increase. The use of setups downloaded to the instruments, and the extensive use of hardware instruction "broadcast" further increase throughput as the number of sites increases. IG-XL V5.0 as we have seen assumes multi-site testing, and all of the test development tools support multi-site development, and automate much of the process. The per instrument clock and PatGen architectures provide the fully synchronized, asynchronous pattern control required for concurrent, multi-site test. With the "every instrument on every pin" philosophy enabled by the DIB Access function and the high per pin functionality, per pin and per site instrument configurations are easily built that fully support multi-site parallel test.

Virtual Test

Test simulation software provides a well-established vehicle for reducing time-to-market by breaking the traditionally serial relationship between the design and test processes. This is achieved by providing the means for test development and debug to begin sooner, prior to the availability of first silicon. By increasing the amount of design and test development overlap, problems can be identified and resolved jointly, before first silicon. Test simulation also provides the test engineers with the ability to learn about device behavior before first silicon. This significantly improves confidence in the test package once first silicon is available, and virtually guarantees that any problems that remain to be uncovered are highly likely to reside in the silicon, rather than the test program. The end result is better silicon sooner, better characterization data sooner, and better test coverage sooner. Teradyne Integra FLEX test simulation software functions identically to the actual Integra FLEX test system. It furnishes an environment where the test engineer can 1) debug both the test program and test patterns, and 2) interact with the IG-XL V5.0 program and debug displays off-line in exactly the same way as he/she does on the tester.

VX Test Simulation Software

On the real test system, a DUT is plugged into a DIB, which is itself plugged into the test head, which is populated with test instruments. Under IG-XL V5.0, instructions and data move between the software and test hardware. The test engineer interacts with the hardware through the test program and software tools. The VX Test Simulation software uses the same IG-XL V5.0 environment, off-line. It mirrors the complete test environment in software on a workstation, keeping the test system free for production testing. The same standard IG-XL V5.0 software environment, running the same test program, using the same tools provides an

identical test development and debug environment without the test system.

Figure 4-29 depicts a block diagram of how the VX environment works. The Test Program and IG-XL V5.0 Tools (blue in the figure) running under IG-XL V5.0 on the workstation are the same as those that run on the production test system. The Design Simulator (green in the figure) is a platform that supports a series of models of the DUT, the DIB, and the Integra FLEX test system. The DUT model is supplied by the design group, while the DIB model is supplied by the test group. The VX Test Simulation software (red in the figure) consists of two primary pieces –1) the ATE instrument models that simulate the behavior of the tester hardware, and generate stimulus and capture responses, and 2) IG-XL V5.0 ExChange, with is a software "bus" that lets the IG-XL V5.0 test program control the instrument models. In operation, there is a continuous flow of events to and from the instrument models. The instrument models generate stimuli to the DUT model, whose response is captured by other instrument models. The response data is sent back to IG-XL 5.0. This is a closed loop test simulation that mirrors the way the actual Integra FLEX test system operates.

Figure 4-31 shows how VX fits into the overall design-to-test flow. The design team creates simulation "test benches" and runs large numbers of simulations to verify various aspects of the new design. Simulations are run with the purpose of generating output that will be used to create test patterns for ATE. The design simulation data is then translated into pattern/timing/format files that can be loaded into ATE. This is done either by using commercial tools that perform this task from companies such as Fluence (TSSI), IMS, and others, or with tools created in-house. The resultant translated files, together with manually coded portions, are combined to produce a test program that can be loaded, which then allows the test engineer to work with IG-XL 5.0.

Once the program is loaded, the traditional approach would require the test engineer to begin debugging the test package on the test system with device silicon. With VX test simulation, the test engineer can debug the test package, without silicon, using the Integra FLEX test system, DIB, and DUT models. Once the pre-silicon debug is

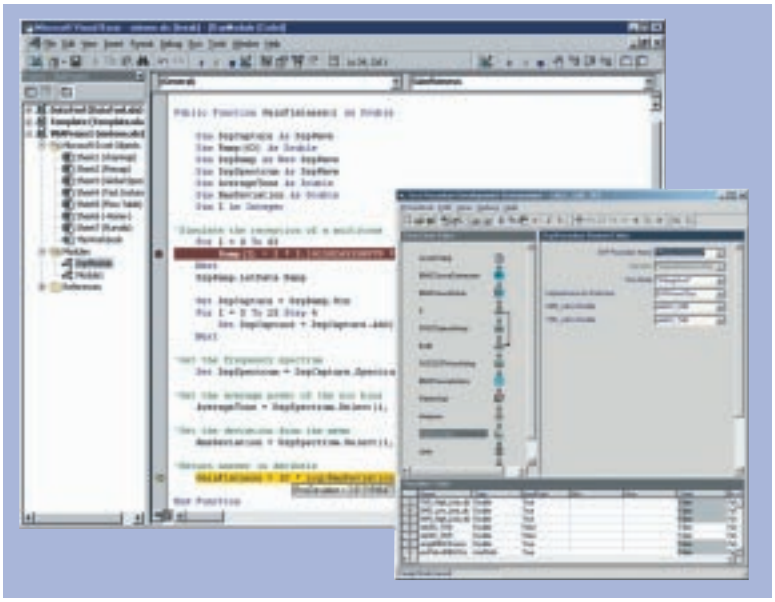


Figure 4-26: DSP environment

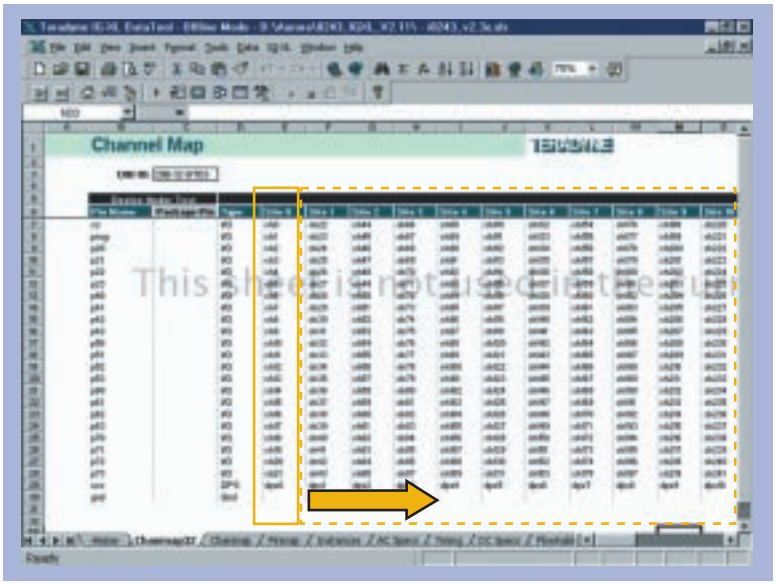


Figure 4-27: Channel map edit for multi-site

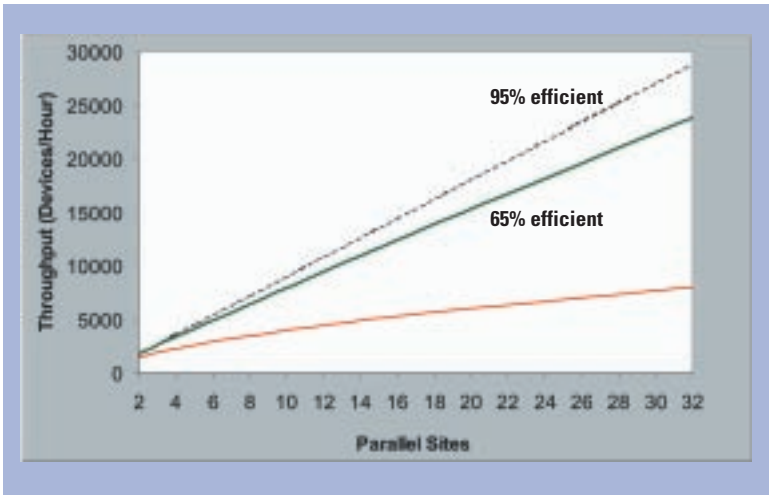


Figure 4-28: Integra FLEX/IG-XL 5.0 multi-site efficiency

completed and silicon is available, test engineering time on the actual test system is much more efficient, and can be used more effectively to characterize the device. Using VX after first silicon is available can be very helpful in analyzing problems and developing new tests that result from working with real silicon.

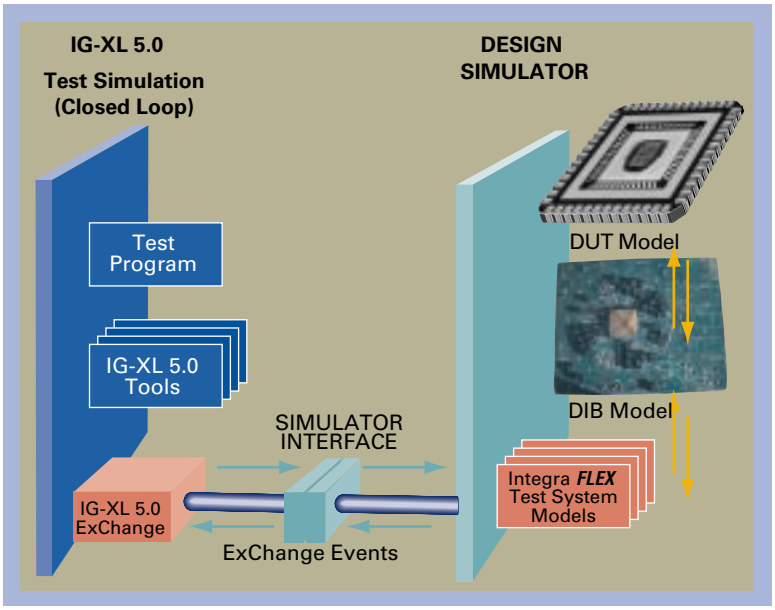


Figure 4-30: The VX test simulation environment

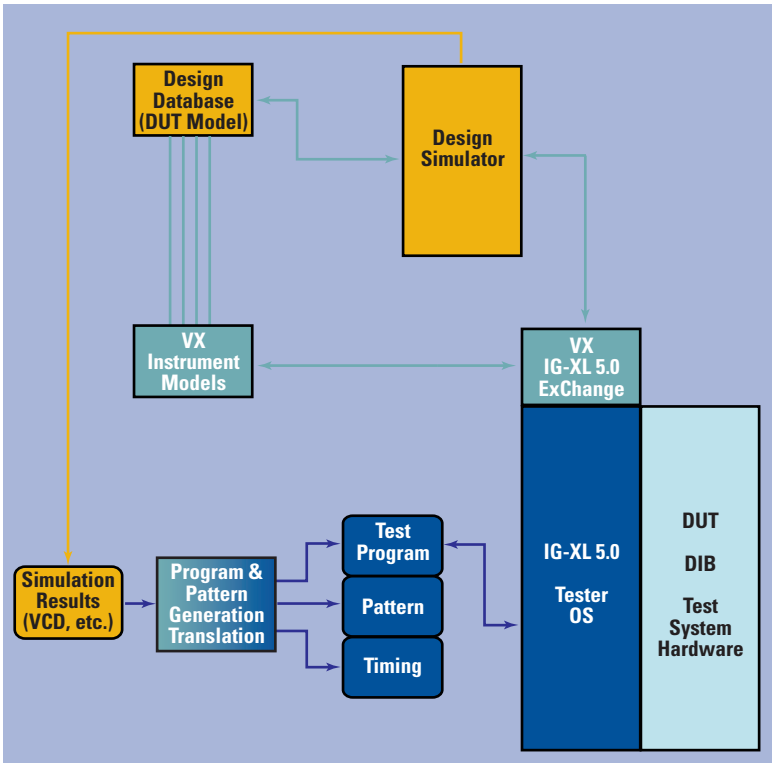


Figure 4-31: VX test simulation in the design-to-test flow

Digital VX

DigitalVX extends the power of test simulation to the pre-silicon debug of both digital test programs and the digital portions of mixed-signal test programs. DigitalVX is provided as an integral part of the Integra FLEX IG-XL V5.0 software, and a single seat does not require an additional license. There are two DigitalVX products:

- VerilogXL version – runs on Cadence Verilog simulator
- ModelSim versions – runs on Model Technology (MTI) Verilog/VHDL simulator

Mixed-Signal VX

There are two VX products for use in mixed-signal test simulation:

- SpectreVX – runs on Cadence Spectre (analog sim.) + Verilog (digital sim.)
- SaberVX – runs on Avanti Saber (analog sim.) + Cadence Verilog (digital sim.)

The VX Test Simulation software is available as a family of products to provide the right level of tools for the problems to be solved. A commitment to Test Simulation requires that the design and test processes be integrated, which requires funding and additional personnel. It also requires a change in the methodology of the organization, which can create resistance to the necessary commitment to this approach. The VX product family enables starting with a less capable tool that requires less change, and progressing to tools that require a larger commitment, but provide larger returns.

qVX

The qVX test simulation product is designed for very large-scale mixed-signal SOC devices. It runs mixed-signal simulations on a digital simulator. The analog components are modeled as real-number transfer functions using digital modeling code. This “pseudo-analog” approach makes very large mixed-signal test simulations run faster because no analog simulator is needed.

Design-to-Manufacturing Support

Teradyne takes the philosophy of working with multiple partners to provide a broad base of design-to-manufacturing solutions. The Integra FLEX test system and IG-XL V5.0 are supported by a network of companies who are leaders in their particular areas of expertise. These resources, with the Integra FLEX and IG-XL V5.0 at its core, collectively provide a fully integrated

design-to-manufacturing solutions.

- Test Simulation
  - Cadence
  - Mentor
  - Synopsys
  - Avant!
  - IMS
- Digital Pattern Translation and Simulation
  - IMS
  - Simutest
  - SourceIII
  - Test Insight
  - TestSpectrum
  - TSSI (Fluence)
- Design For Test
  - Mentor
  - Synopsys
  - LogicVision
- Test Optimization
  - Galaxy

Section 5

Instrument Description and Specifications

Common Instrument Functionality

Integra FLEX instruments provide both high pin and functional density to aid in the breakthrough economics of the Integra FLEX Test System. Along with the high pin and functional densities, each instrument has resident, redundant resources to help eliminate tester bottlenecks so that multi-site throughput is maximized, and in fact, can execute with minimal incremental additional execution times over single-site test times. Finally, every instrument — AC, DC, Microwave and Digital — has identical Direct Digital Synthesis Clock, PatGen, PSET Memory, Time Measurement Unit, (DC instruments only) per pin PMU, (DC & AC instruments) DIB Access, and back-end high speed data bus subsystems, all of which provide pattern-synchronized, simultaneous instrument setup, capture, and data move-while-capture. All instruments within the test head, again — AC, DC, Microwave, and Digital — can be triggered from one another, and are pattern step-locked to one another, allowing rapid test pattern debug across ***all*** DUT functions. The contribution of each of these subsystems to tester throughput is briefly described in the following sections. The specific capabilities of each instrument are described later in this section.

Any instrument can be located in any of the 24 universal instrument slots within the Integra FLEX test head. Each instrument provides a DIB interface tailored to its particular function, so that digital, analog, dc, or microwave signals are suitably terminated at the pogo pin header of the instrument. This provides a significant reduction in DIB complexity, reducing DIB development time, as does DIB Access which is described in a following section. The ability to put any instrument in any slot means that the Integra FLEX test head can be configured to accommodate the majority of devices to be tested with only DIB changes and test program loading.

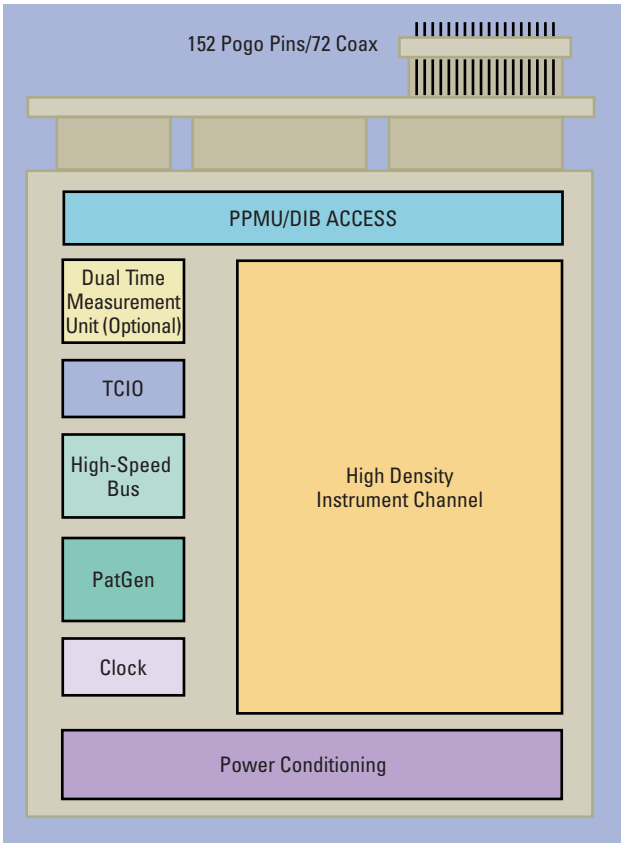


Figure 5-1: Integra FLEX instrument functional block diagram

Instrument Triggering

One of the many capabilities designed into all aspects of the Integra FLEX test system involves the flexibility available to trigger instrument captures. Instrument architecture is such that captures or measurements can be initiated through any one of four sources – from the test pattern, from another instrument, from the tester computer, or from the DUT itself. Instruments can "listen" to a variety of signal sense lines for capture/measurement triggers. This capability provides significant closed-loop testing abilities that can enable rapid multi-site, concurrent device testing.

Per Pin Measurement Unit

Each input and output pin on all AC and Digital instruments has a dedicated Pin Measurement Unit to eliminate shared resource bottlenecks. Each PPMU can force current and measure voltage or vice versa, with 1% accuracy over a -1 V to +6 V and 2 mA range. Per pin measurement units on all AC and digital pins, plus the inherent V/I capabilities of the DC instruments, allows simultaneous continuity and leakage measurements for all DUT pins.

DIB Access

DIB Access provides the capability to route signals from one instrument to another, without requiring DIB application relay circuitry. The DIB Access feature also provides a modulation input for the DC instruments so they can be driven from the AC instruments for high power modulated source requirements, and also, acts as an output from the High Voltage Front-end (see following section). To illustrate how DIB Access works to reduce the amount of DIB circuitry required, consider the case of a DUT consisting of an ADC with a 3:1 differential multiplexer front-end. Refer to Figure 5-2.

If we assume the test requirement is to measure DC resistance on all six input lines, and then inject an AC signal to all three differential inputs through to the ADC for analysis, Figure 5-2(a) depicts the application circuitry required to perform this test without the Integra FLEX DIB Access feature. Twelve relays are required on the DIB to route the AC signal source to the each of the differential inputs to the multiplexer. Figure 5-2(b) shows how the relays are no longer required in the same test situation in the Integra FLEX test system. The AC signal source is routed from the AC instrument to the DC instrument(s) within the instrument DIB Access subsystem, reducing the amount of application circuitry and the effort required to design it. Figure 5-2(c) shows how AC and DC capability are provided behind every DUT pin using the DIB Access feature.

Direct Digital Synthesis Optical Reference Clock

Clock architectures typically rely on a master frequency synthesizer with 1 Hz resolution that is divided by a series of integer dividers to generate divide-by-N and divide-by-X

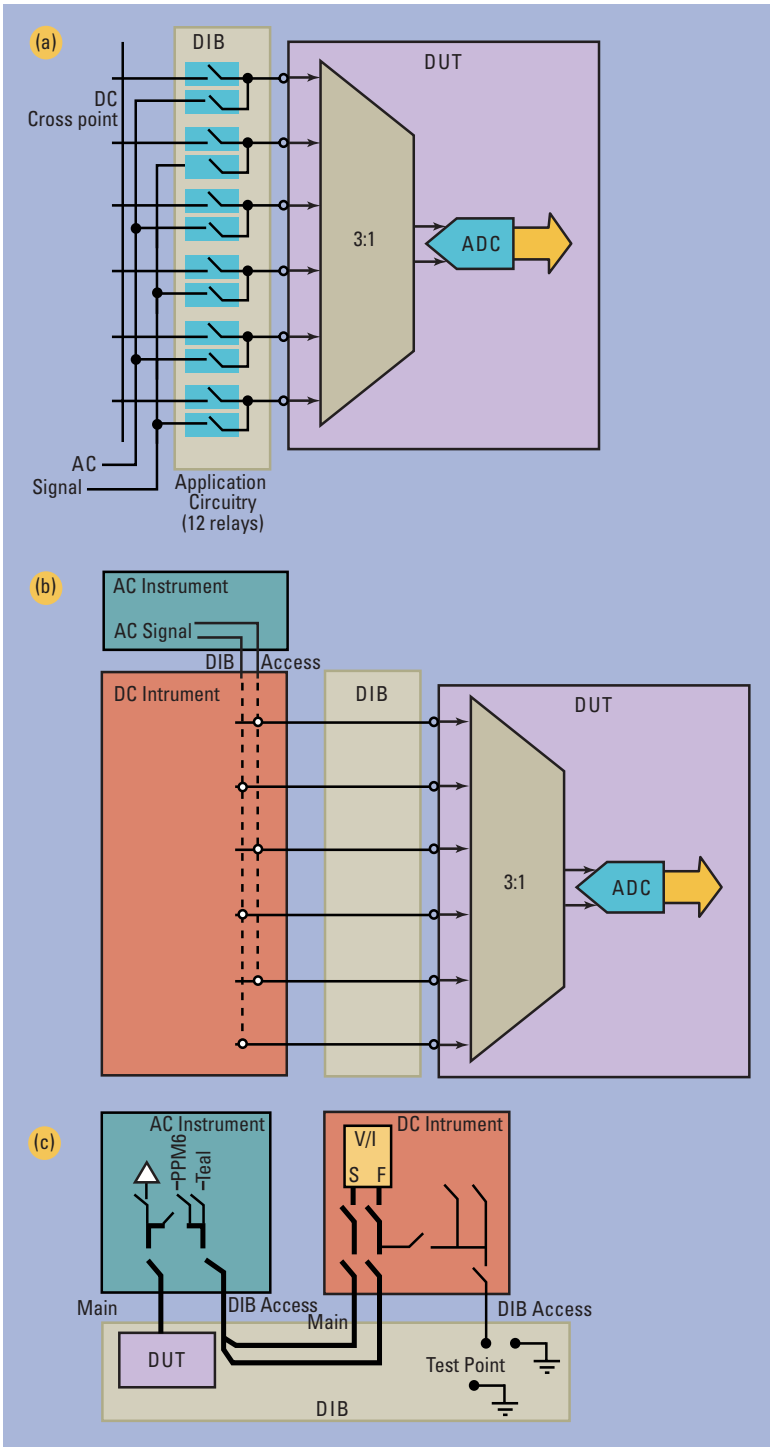


Figure 5-2: DIB access

Time Measurement Unit Feature	Specification	Accuracy
High Voltage Front-end		
Input Voltage		
DC30 Instrument	0 to ±30 V	
DC75 Instrument	0 to ±75 V	
DC90 Instrument	0 to ±200 V	
Time Stampers		
Resolution	1 ns	2 ns
Range	670 ms	

Table 5-1: Time measurement unit specifications

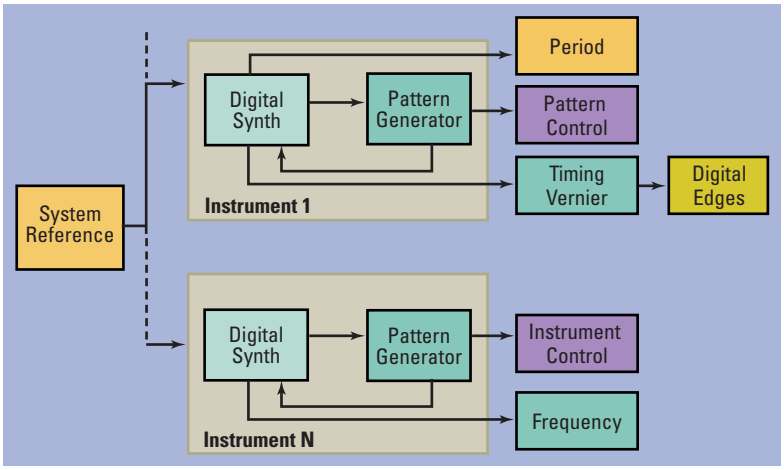


Figure 5-3: Integra clock architecture

clock signals for driving the DUT. These two clock signals are coherent and perfectly related to one another by an integer value. The inherent problem with this approach is that division by something other than an integer value isn't possible, and, as the reference frequency increases, the difference between division by two successive integers also increases, resulting in loss of resolution. Further, it is the ratio of F_{TEST} and F_{CLOCK} that must be precisely defined so that test time is minimized, accuracy and repeatability are as high as possible, the device specifications are met, and ultimately, all four of these factors are satisfied, preferably without compromise.

To accommodate the needs of analog, digital, and mixed-signal testing in varying test environments ranging from DFT to mixed-signal SOC, the Integra FLEX clock architecture on every instrument allows the test engineer to find the optimal combined solution for minimum test time, highest possible measurement accuracy, and lowest possible repeatability errors, with no compromise in device specifications. Integra FLEX represents the 4th generation of clock architecture utilizing a Direct Digital Synthesis Optical Reference Clock per instrument. Each instrument now has it's own 29-bit direct digital synthesis optical reference clock. The 29-bit direct digital synthesis clock provides <1.0pp-billion frequency ratio accuracy. Any required clock frequency can be generated, with a resolution of 36 atoseconds. The clock on each instrument is completely independent from those on other instruments so that individual instruments can run asynchronously with respect to each other, yet all clocks are referenced to a common precision 100 MHz system reference clock, which allows all instruments — AC, DC, Microwave, and Digital — to be fully time synchronized to one another. A Mixed-Signal Workshop tool is provided that enable the test engineer to set the device specifications and to know what the limits of tester performance will be, before any tests are run. This has significant impact on mixed-signal device testing, and can benefit digital and linear testing through improved clock accuracy as well. Refer to Figure 5-3.

With a clock on every instrument, timing and events can be very accurately controlled across all instrumentation. Because each clock is essentially a 29-bit counter synchronized to the master system reference, and with all starting at "zero" at t_0, the timing relationships among all clocks (instruments) are precisely known from one clock "tic" to the next, throughout every test. The time and phase for all instruments — AC, DC, Microwave, and Digital — can therefore be accurately tracked. A time domain tool is provided which allows the test engineer to look at all analog and digital events together, with all timing relationships accurate to 36 atoseconds. Because the settling time of the analog instruments are precisely known for example, the problems of minimum test time and measurement accuracy can be solved because the actual timing of all events can be precisely lined up. Settling times of analog instruments, for example, can be adjusted to start at the proper time so measurements are valid at the precise point in time when they need to be. The test execution time can therefore be as fast as it can be. Refer to Figure 5-4.

Pattern Generator

The Pattern Generator (PatGen) controls local events and instrument setups. Every instrument — DC, AC, Microwave, and Digital — has its own PatGen driven from the instrument's clock subsystem. This means that all instruments, ***including analog, are controlled from the pattern***. Each instrument can run asynchronously, at an independent rate dictated by the IP core within the DUT it is to test, yet all patterns are synchronized because the instrument clocks themselves are synchronized. Patterns can therefore exercise any device, not just digital. This capability allows the Integra FLEX to concurrently test multiple IP cores, and their interactions, under actual device operating conditions.

An example of how this concurrent IP core test capability can reduce test time by 43% is shown in Figure 5-5. A wireless baseband device has two primary IP cores — a codec which runs at 8 kHz, and an RF/IF section operating at 9.72 MHz. The device is meant to be used while talking and listening (8 kHz) and transmitting and receiving (9.72 MHz) are happening simultaneously. To verify that no core interactions occur, both must be tested concurrently. The benefit of this concurrent test, aside from uncovering interactions among the cores, is that the total test time is reduced.

Logical PatGens

The Integra FLEX instruments allow multiple independent instrument PatGens to be grouped together, up to eight (8) asynchronous clocks ***per site***. This provides the maximum flexibility required for true linear and mixed-signal IP-core testing. Up to five (5) logical PatGens can be created across multiple instruments — AC, DC, Microwave, and Digital.

PatGen Failure Reporting

The capability to concurrently test multiple IP cores, and their interaction, under actual device operating conditions is of little use if the concurrent test can't be debugged. With multiple PatGens on different types of instruments running asynchronously at different rates, if a failure should occur in one core, all PatGens must be able to stop so that their exact position in their respective patterns is known. Without knowing the exact position within the pattern of every instrument — AC, DC, Microwave, and Digital — debugging the concurrent test is impossible. Failures are time stamped, so all PatGens can "line up" on a time stamp. Each PatGen on each Integra FLEX instrument can communicate failures with each of the other instruments, so they can all respond to Halt-on-Fail conditions, with all events across all PatGens/instruments precisely aligned. The ability to perform debugging is built-in to the Integra FLEX hardware.

Parameter Set Memory

Closely allied with the PatGen on each instrument is the Parameter Set (Pset) memory subsystem. The Pset memory allows multiple analog instrument setups to be downloaded to each instrument and stored for later use. When the test pattern executes, each instrument setup is referred to ***by name***, so instrument setup is controlled locally on each instrument, from within the test pattern. This ensures that all instruments are available for test execution as quickly as possible, improving overall test throughput.

Capture Memory

Each Capture instrument has a large block of dynamically assigned capture memory, which varies in depth depending on the particular instrument. The memory is structured such that data from one capture can be moved out concurrently with the capture of data from the next test. Sufficient memory is available for storage of still additional captured data if necessary.

High-Speed Back-end Data Bus

At the completion of a data capture, each instrument independently initiates a move of the captured data for processing. This data move occurs independently and simultaneously with instrument setup from PSET memory and the start of the next test. The data moves off each instrument on its own high-speed bus to await processing.

TCIO Bus

Each instrument receives test instructions, timing, PSET data, and other test execution data from the test computer through the Teradyne-proprietary TCIO bus. In addition, multiple instruments can be triggered from TCIO using a single write command. This could be used to trigger 20 V/I meters each on four DC30 instruments, for example, and would result in 80 simultaneous measurements, under test program control, from a single instruction.

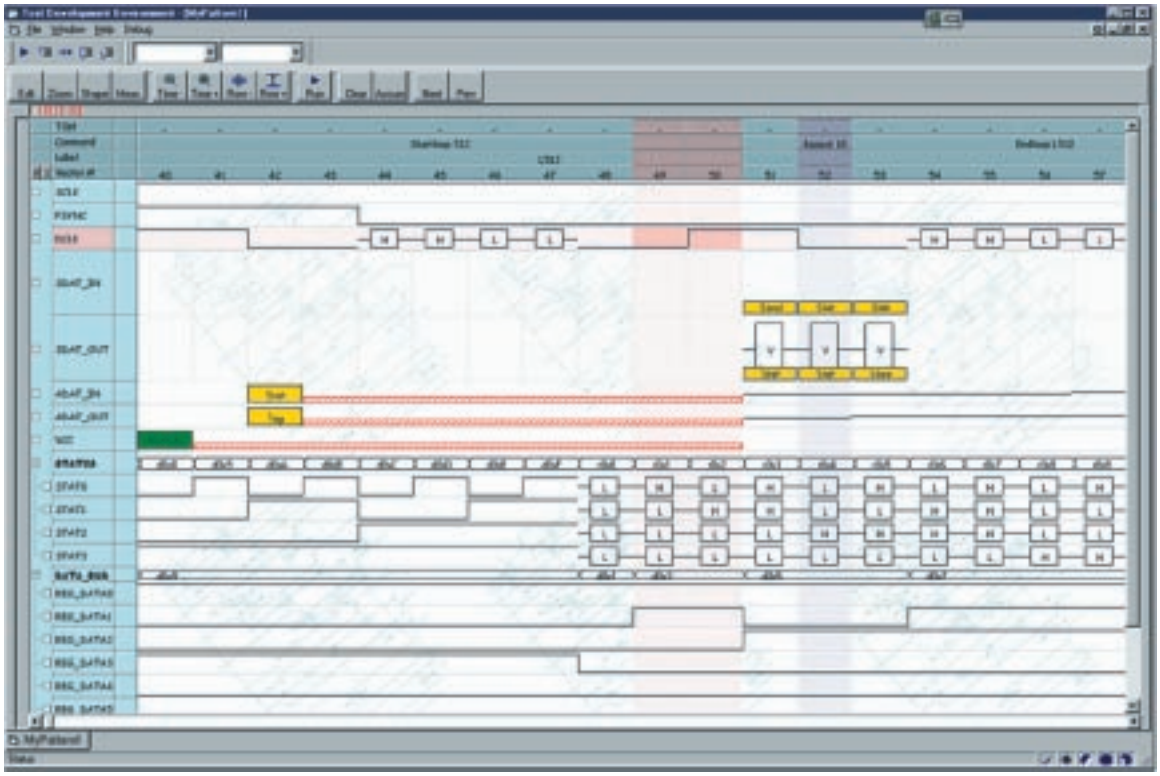


Figure 5-4: Time domain tool – synchronized analog and digital events

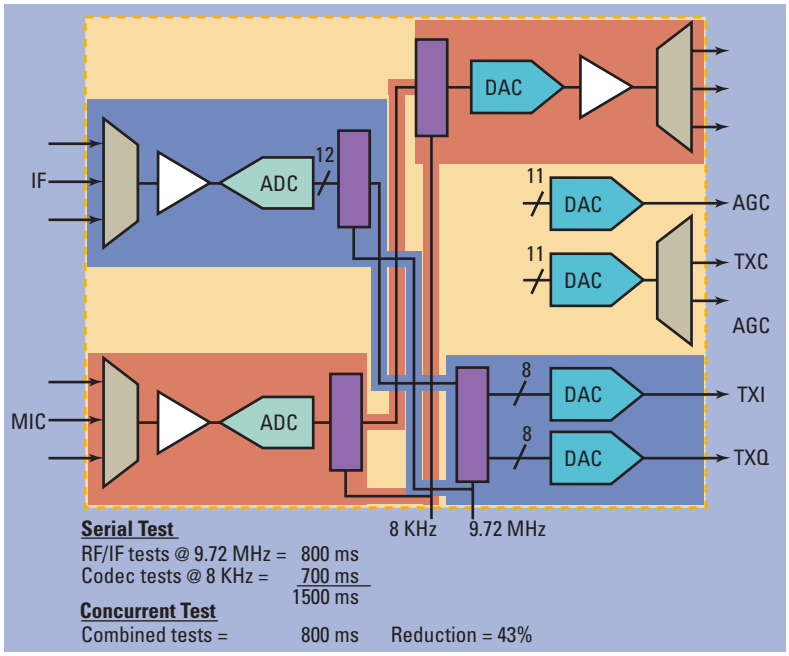


Figure 5-50: Integra FLEX concurrent IP core testing

Armed with the foregoing suite of common functional blocks, each instrument adds its own specific set of capabilities as described in the following sections.

The DC instruments consist of three V/Is – theDC30, DC75), and DC90. All are true four quadrant V/Is, each with a different number of channels and voltage and current ratings. All V/Is can force voltage/measure current, force current/measure voltage, force voltage/measure voltage, or force current/measure current. The architecture of all three DC instruments is the same, as is the programming methodology. There are common functions among the three DC instruments in addition to those shared by all Integra FLEX instruments. These common functions are described in the next section.

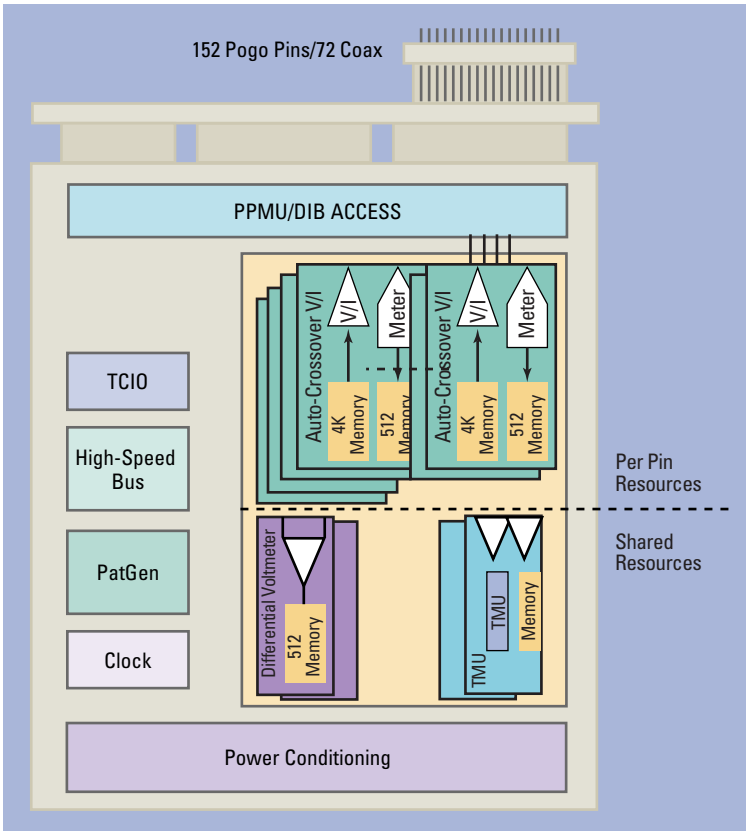


Figure 5-6: Common DC instrument functions

Common Functionality

Figure 5-6 illustrates the common features available on each DC instrument. All V/Is are four quadrant, auto-crossover designs, with ranges spanning the full capability of each instrument. Each V/I channel has local source and capture memory. The DC30 and DC75 have shared resources including two differential voltmeters, each with their own capture memory, DIB Access, internal switching from per channel resources, and Time Measurement Units (TMU). The DC90, as a floating instrument, provides differential metering capability via its local channel meters. It also incorporates DIB Access, internal switching, and TMU functionality.

V/I Modulation

Each V/I channel has its own source memory for driving the DUT with ramps, steps, and other dynamic waveforms. In addition, the DIB Access feature on each instrument can be used to enable the DC instruments to accept a modulation input from an analog instrument, such as an AWG. This feature allows an AWG instrument to drive DUT inputs with higher power modulated signals than it could drive on its own in some cases.

Time Measurement Unit

Every DC instrument has one or more Time Measurement Unit (TMU) subsystems. The TMU provides the means to tag events with a very precise digital count referenced to another event. The TMU is accurate to within ±2 ns, with resolution slightly better than 1 ns. The TMU consists of two parts. The first is a High-Voltage Front-end, which provides sense line multiplexing, attenuation and termination for signals up to the maximum voltage of the instrument, and outputs a standard TTL signal, when needed, to the Time Stampers. Each HV Front-end has two high performance signal paths. The second part

of the TMU is a dual Time Stamper, which performs the tagging of events with a digital count.Each TMU has its own memory. The TMU 1) can look for events from the test pattern, 2) can be gated from the test pattern (i.e. “only look for events within this window”), from any instrument, or 3) can accept events from the DUT itself. Using the Time Stampers, parallel multi-site tests can be performed for rise/fall times, propagation delay, pulse width, frequency, and period.

Table 5-1 summaries the key specifications for the Time Measurement Unit.

Time Measurement Unit		
Feature	**Specification**	**Accuracy**
High Voltage Front-end		
Input Voltage		
DC30 Instrument	0 to ±30 V	0.05%
DC75 Instrument	0 to ±75 V	0.05%
DC90 Instrument	0 to ±200 V	
Time Stampers		
Resolution	1 ns	2 ns
Range	670 ms	

Table 5-1: Time measurement unit specifications

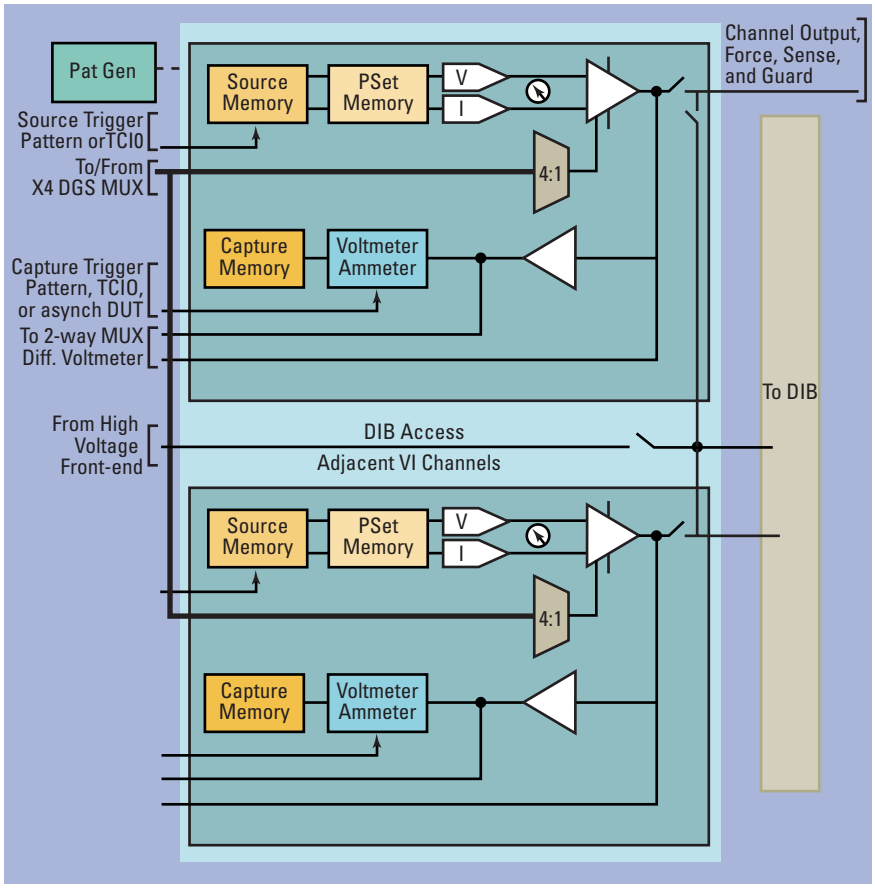


Figure 5-7: DC30 instrument block diagram

The DC30 instrument has 20 V/I channels, each of which has a 2.5K sample Arbitrary Waveform Generator (AWG) for voltage or current source, and its own meter with 512 sample capture memory. There are two High Voltage Front-end subsystems on the instrument, as well as two, Dual Time Stampers. Four (4) Digital Ground Sense (DGS) lines are provided per DC30 instrument to support multi-site measurements referenced to each DUT. The DC30 is a ground-referenced V/I. Table 5-2 summarizes the key DC30 instrument specifications.

Figure 5-7 depicts a block diagram of the DC30 instrument. Figure 5-8 depicts the compliance points of the DC30 instrument.

DC30 V/I Instrument Feature	Specification	Accuracy
Independent V/Is	20	—
Per Channel Meters	20	—
V/I Source Memory	2.5k samples	—
Meter Capture Memory	512 samples	—
Differential Voltmeters	2, fully matrixed	—
Input Voltage	±5 V differential	
Common Mode	±30 V	
High Voltage Front-ends	2	—
Input Voltage	0 to ±30 V DC	
Time Measurement Units	2, dual Time Stampers	
V/I Output		
Voltage	0 to ±30 V DC	±0.05%
Compliance	10 V @ 200 mA DC	
	30 V @ 100 mA DC	
Current	±200 mA, metering	±0.1%

Table 5-2: DC30 V/I specifications

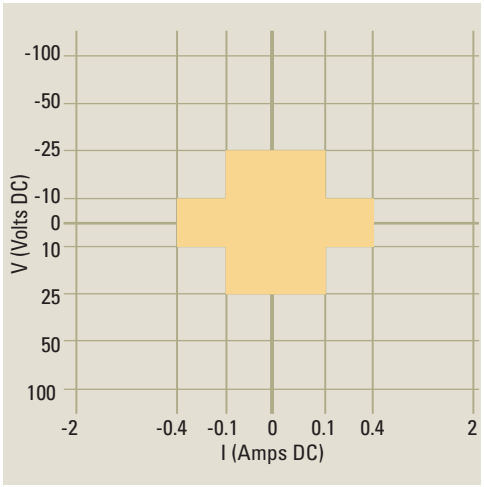


Figure 5-8: DC30 compliance points

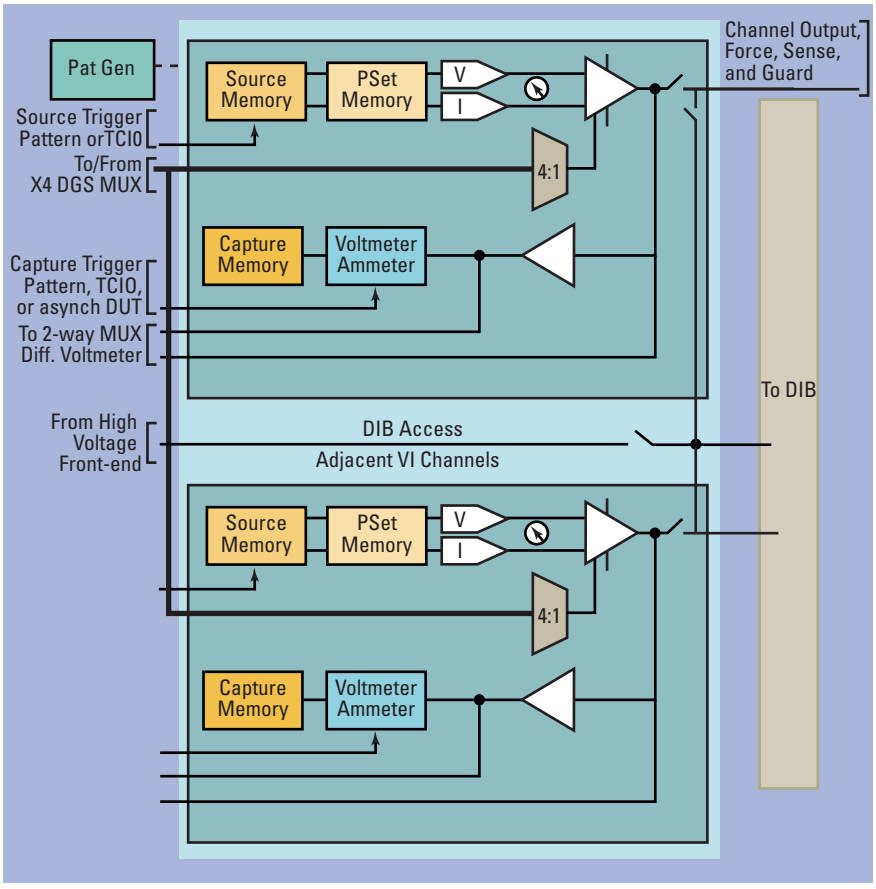


Figure 5-9: DC75 instrument block diagram

The DC75 instrument has 4 V/I channels, each of which has a 2.5K sample Arbitrary Waveform Generator (AWG) for voltage or current modulation, and its own meter with 512 sample capture memory. There are two High Voltage Front-end subsystems on the instrument, as well as two, Dual Time Stampers. The DC75 is a ground-referenced V/I. Four (4) Digital Ground Sense (DGS) lines are provided per DC75 instrument to support multi-site testing, with all measurements referenced to the DUT. Table 5-3 summarizes the key DC75 instrument specifications. Figure 5-9 depicts a block diagram of the DC75 instrument. Figure 5-10 depicts the compliance points of the DC75 instrument.

DC75 V/I Instrument		
Feature	**Specification**	**Accuracy**
Independent V/Is	4	—
Per Channel Meters	4	—
V/I Source Memory	2.5k samples	—
Meter Capture Memory	512 samples	—
Differential Voltmeters	2, fully matrixed	—
Input Voltage	±5 V differential	
Common Mode	±75 V	
High Voltage Front-ends	2	—
Input Voltage	0 to ±75 V DC	
Time Measurement Units	2, dual Time Stampers	
V/I Output		
Voltage	0 to ±75 V DC	±0.05%
Compliance	6 V @ 2 A DC	
	15 V @ 1.2 A DC	
	75 V @ 350 mA DC	
Current	±2 A DC, 1 µA metering	±0.1%
	<35 mV/A regulation; high regulation mode	

Table 5-3: DC75 V/I specifications

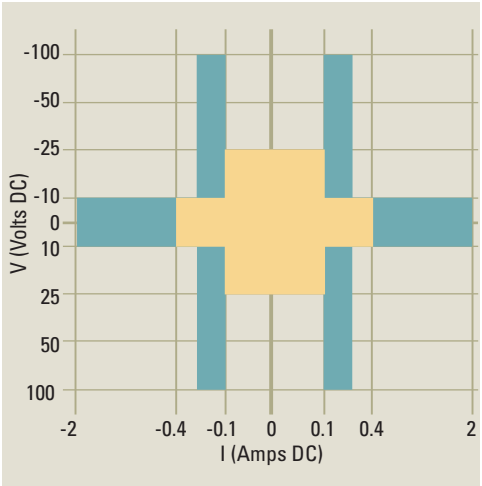


Figure 5-10: DC75 compliance points

Special DC Instrument Mode

DC30/DC75 Device Power Supply/High Regulation Mode

For applications that require delivered at a stable voltage, such as digital logic, both the DC30 and DC75 can operate as Device Power Supplies (DPS). In the DPS, or high regulation mode, the V/Is can maintain load voltage regulation to ±35 mV, with the output load current varying by up to (one) 1 Ampere. Any number of V/Is on each instrument can be configured independently to operate in the DPS mode, while the remainder operate as standard V/Is or in high impedance mode.

DC30/DC75 Merge Mode

The DC30 and DC75 instruments can operate in what is referred to as the Merge Mode, which eliminates the difficulties of programming and sequencing multiple power supplies that are connected in parallel to provide more current that a single instrument can provide. Under direct test program control two adjacent V/I channels can be configured for the Merge mode, which effectively ties their outputs together internally. When merged channels are defined in the Channel Map, the control logic for one of the V/I is turned off, allowing a single set of control logic to control both V/I outputs. From a programming viewpoint, the merged pair are treated like a single V/I with higher current range available for selection, even though physically two V/I channels. Parallel wiring is not required at the DUT; the parallel connections are handled internally to the V/Is. The Merge mode only works with adjacent V/I pairs. If even more current is required, two merged mode V/I pairs can be merged traditionally at the DUT.

DC90 V-I Source

The DC90 instrument is a four (4) channel V/I, each of which has a 4K sample Arbitrary Waveform Generator (AWG) for voltage or current output, and its own meter with 4K sample capture memory. The DC90 channels are independantly isolated and floating. There are High Voltage Front-end sub-systems on the instrument, as well as two (2), Dual Time Stampers. Rail power supplies can be set for symmetric or asymmetric rail voltages up to 180 V. Two DC90 instruments can be connected in series for a total output voltage of 250 V. Table 5-4 summarizes the key DC90 instrument specifications. Figure 5-11 depicts a block diagram of the DC90 instrument. Figure 5-12 depicts the compliance points of the DC90 instrument.

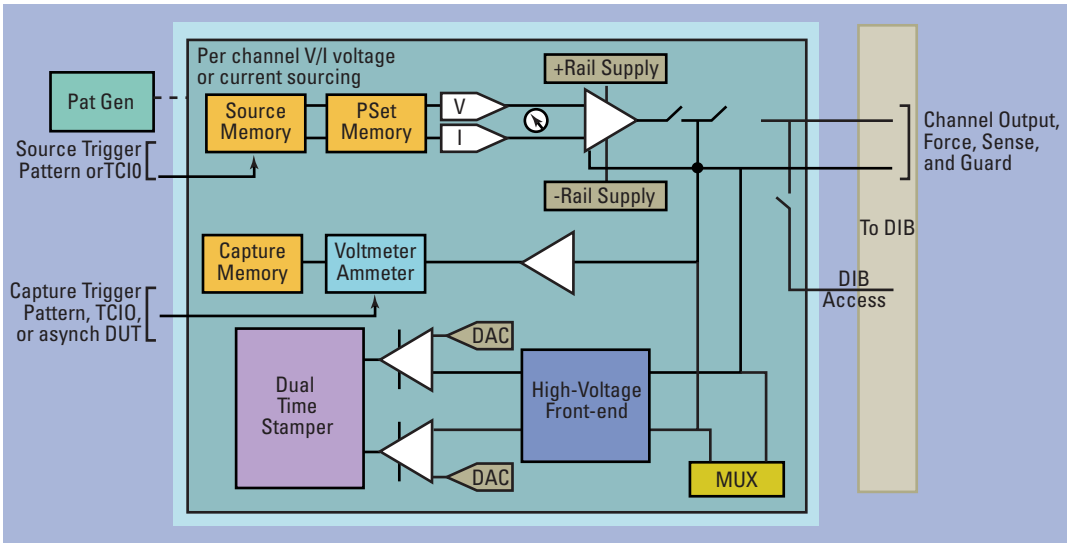


Figure 5-11: DC90 instrument block diagram

DC90 V/I Instrument Feature	Specification	Accuracy
Independent V/Is	4	—
Independent Meters	4	—
V/I Source Memory	4k samples	—
Sample Rate	1 S/ms to 1kS/ms	
Meter Capture Memory	4k samples	—
Sample Rate	10kS/s, 50kS/s, 100kS/s	
High Voltage Front-ends	4	—
Input Voltage	0 to ±200 V DC	
Time Measurement Units	4, dual Time Stampers	
V/I Output		
Voltage		
Four quadrant	±90 V DC	
Single quadrant	0 to 180 VDC	
Compliance		
Continuous	25 V @ 2 A DC	
	50 V @ 1 A DC	
	90 V @ 500 mA DC	
	180 V @ 250 mA DC	
Pulsed	25 V @ 10 A DC	
	50 V @ 10 A DC	
	90 V @ 2 A DC	
	180 V @ 500 mA DC	
Current	±2 A DC, 50 µA metering	
	±10 A DC pulsed (2 ms, 10% duty cycle)	
	35 mV/A (pk) regulation; high regulation mode	

Table 5-4: DC90 V/I specifications

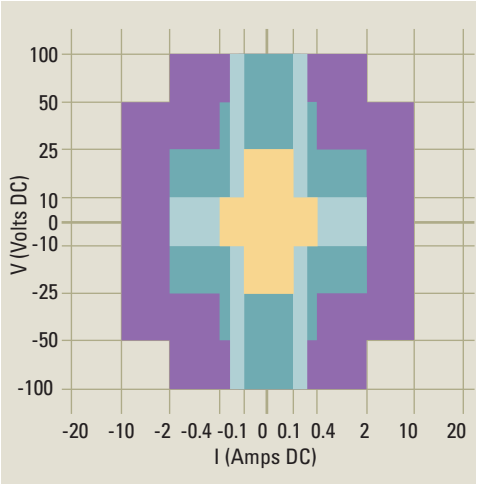


Figure 5-12: DC90 compliance points

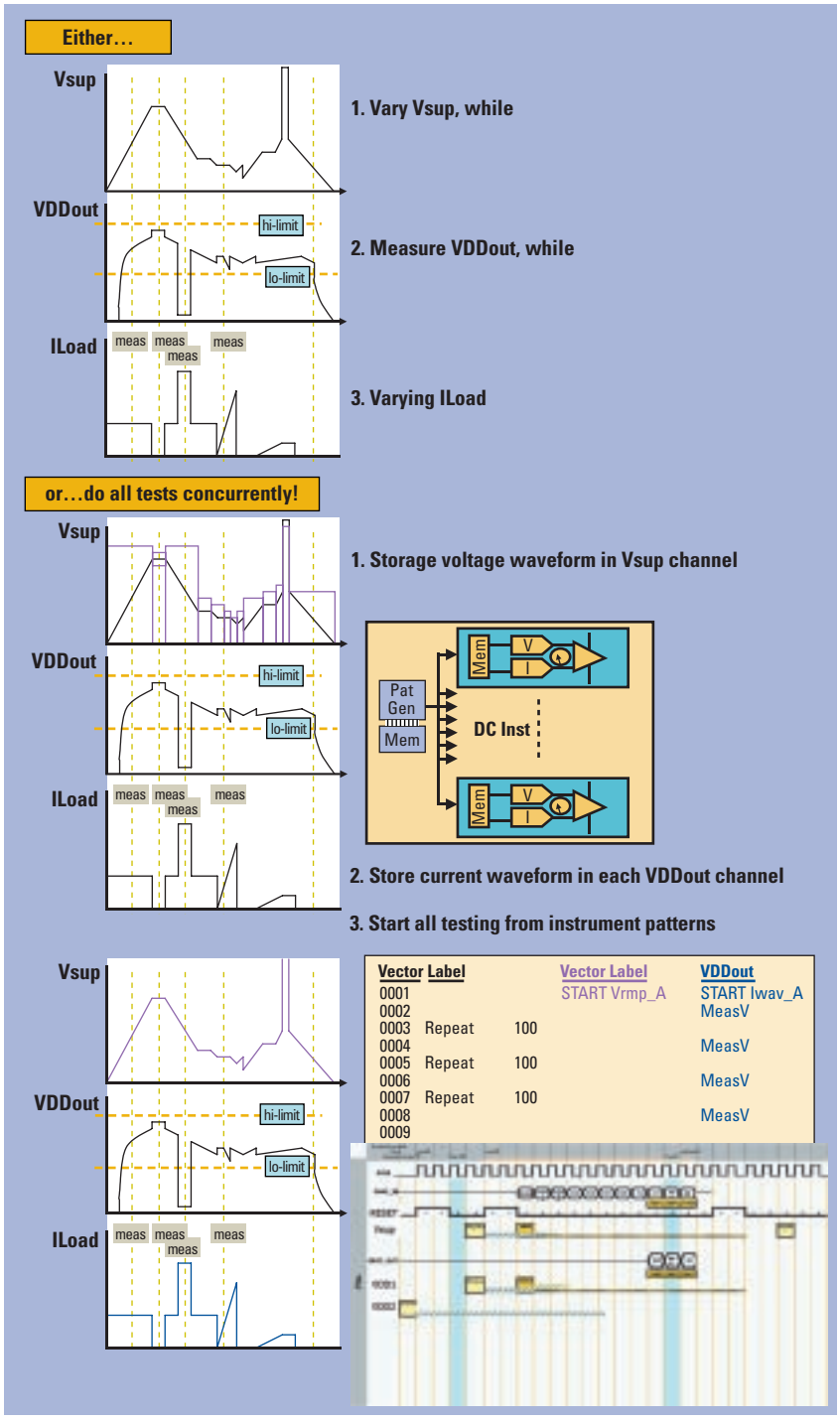


Figure 5-13: Simultaneous line/load regulation testing

To illustrate the potential test execution time reductions possible with the capabilities of the Integra FLEX DC instrument architecture, consider the test problem of a linear voltage regulator. A three-terminal device, the voltage regulator accepts varying voltage from a battery and must provide a well-regulated output voltage, despite load current variations. The test problem is to measure both line and load regulation of the device. A straight-forward test approach would be to do these tests in series — that is, to first vary the input $V_{BATTERY}$ and measure the V_{OUT} (line regulation), then vary the I_{OUT} and measure V_{OUT} (load regulation). Integra FLEX DC instruments allow both tests to occur simultaneously. As shown in Figure 5-13, two V/Is are used, one for the input to the regulator, one on the output. The input voltage and output current waveforms are stored in their respective source memories, and both sources are started at the same time from the pattern. Measurements on both line and load regulation are captured at the same time. The device is tested as it is used.

AC Instruments
Broadband AC Instrument (BBAC)

BBAC Instrument Feature	Specification
Independent High Precision AWG Sources	
Quantity	1 or 2; note 1
Maximum Sample Rate	1 Gsps
Output	
Maximum AC Voltage	±2.56 Vpk
Configuration	Differential
Impedance	50 Ohms
DC Offset	±8 V, programmable
Programmable Common-mode	+5.0 V/-2.5 V
DC Voltage Accuracy	0.1%
Independent High Precision Capture Instrument	
Quantity	1 or 2; note 1
Resolution	24 bits
Maximum Sample Rate	50 Msps
Input	
Maximum Voltage	±8 Vpk
Configuration	Differential
Impedance	10 M Ohms
Coupling	AC or DC
DC Offset	±6 V, programmable
DC Voltage Accuracy	0.1%
Bandwidth (note1)	3.0 or 15 MHz
Noise Density	-150 DBfs/Hz; note 2

Notes: 1. Software licensed
2. 10 kHz to 15 MHz

Table 5-5: BBAC instrument

The Broadband AC instrument (BBAC) is a source/digitizer pair providing noise density performance of -150dBfs/Hz over a 15 MHz bandwidth. Depending on the software license, the BBAC can be implemented as a single or dual source. In the dual source/capture implementation, both high precision Arbitrary Waveform Generators (AWG) and Digitizers are completely independent. The BBAC is equipped with PPMU on all pins.

The BBAC's performance is accomplished by fixing the sampling rate of the on-board converters and optimizing their frequency and amplitude performance. To accommodate the need for varying the sampling rate for a specific waveform capture from the DUT, the BBAC instrument uses hardware DSP to provide a real-time conversion from the test engineer-specified sample rate to the fixed sample rate of the instrument. This conversion is completely transparent to the test engineer, the test program, and the DUT. Table 5-5 summaries the key BBAC specifications. Figure 5-14 depicts the BBAC instrument block diagram. Figure 5-16 depicts the wideband AC source and digitizer performance.

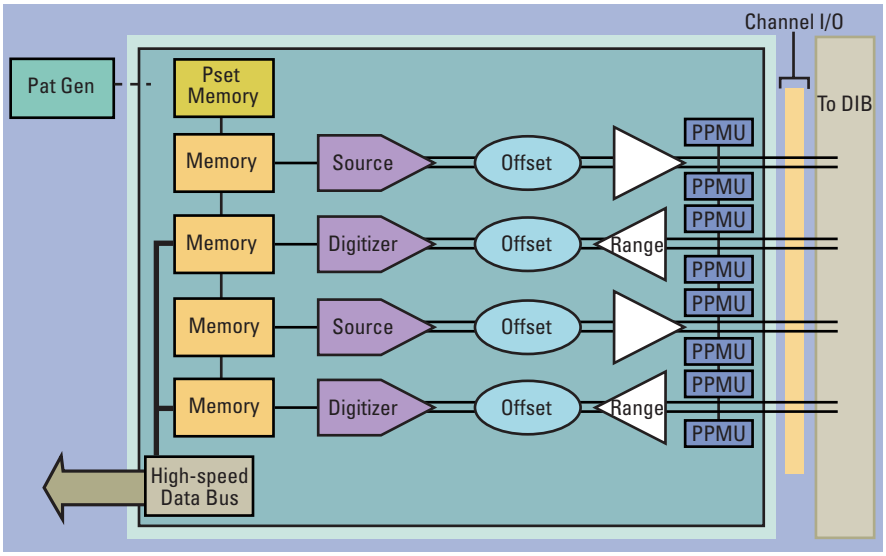


Figure 5-14: BBAC instrument block diagram

VHF AC Instrument (VHFAC)

The Integra Flex VHF AC Instrument (VHFAC) is a complete VHF, video test option with two Source, two Capture, mid-performance TMU, Serial Bus, and Trigger Control instruments, which fits into a single testhead slot. Source, capture, and TMU instruments are all independent, and varying combinations of these instruments can be enabled with software licensing.

The VHFAC Source instrument is a high speed arbitrary waveform generator (AWG) that also has synchronized video event timing lines. The two source channels on each VHFAC are precisely phase matched, enabling waveforms such as I&Q signals to be sourced to the DUT.

The VHFAC Capture instrument is a high speed digitizer that has four input modes: High Resolution, High Speed, Undersampling, and Peak Detect.

Each source and capture instrument has single-ended and differential modes, selectable AC/DC coupling, banks of selectable filters, and multiplexed ports. The VHFAC is equipped with abundant PPMU resources. Table 5-6 summarizes the key VHFAC specifications. Figure 5-16 depicts the VHFAC instrument block diagram.

VHF Source/Digitizer Instrument	
Feature	**Specification**
Independent High Precision AWG Sources	
Maximum Number Per Board	2
Resolution	14 bits
Maximum Sample Rate	400 Msps
Pattern Memory	8 MSamples
Analog Bandwidth	DC - 160 MHz
Output	
Maximum AC+DC Voltage	+/-4 V peak
Configuration	Single-end or Differential
Impedance	50 Ohms
DC Offset	+/-2 V, programmable
Event Timing	
Event Lines	8
Event Memory	2 MSamples
Channel Phase Matching	0.1 degree @ 50MHz
Independent High Precision Digitizers	
Maximum Number Per Board	2
Capture Memory	1 MSamples
Mode	
High Resolution	14 bits, 80 Msps
High Speed	12 bits, 125 Msps
Undersampling	14 bits, 300 MHz
Peak Detect	14 bits, 100MHz
Input	
Voltage Range	8 mV to 8 V peak
Configuration	Single-end or Differential
Impedance	50 Ohms or 10 K Ohms
DC Offset	+/-8 V, programmable
Independent Time Measurement Unit	
Maximum Number Per Board	1
Functions	Frequency, Period, Rise and Fall Times, Propagation Delay, Event Capture, Jitter, etc.
Resolution	2.44ps Nominal
Accuracy	30ps
Input	
Maximum Frequency	400 MHz
Configuration	Single-end or Differential
Impedance	50 Ohms

Table 5-6: VHFAC instrument

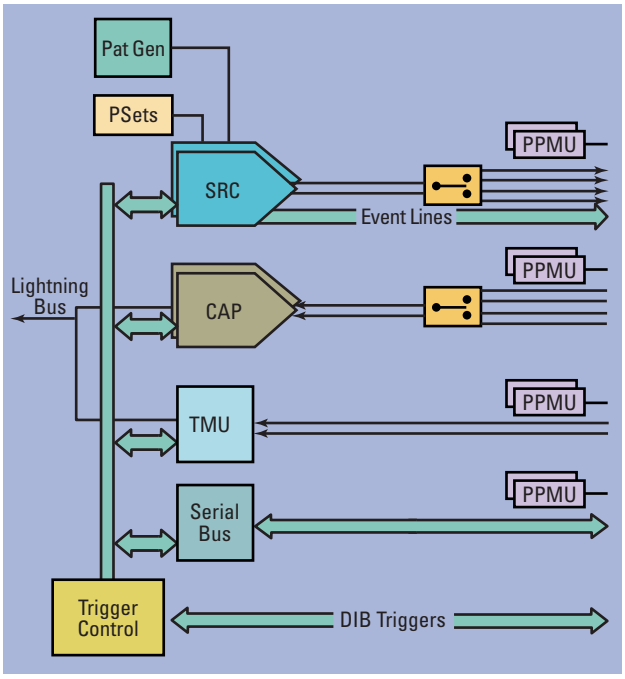


Figure 5-16: VHFAC instrument block diagram

The Integra FLEX microwave instrument suite provides a significant leap in flexibility over traditional RF ATE. The microwave suite is a fourth generation design that consists of Source, Measurement, and Receiver instruments per microwave instrument set. The instrument architecture leverages high performance frequency synthesizer technology to up to four test sites simultaneously, yet allows precision leveling of each instrument-DIB-DUT signal path for maximum test repeatability and throughput. Figure 5-17 illustrates the block diagram of the microwave instrument suite.

The microwave instruments feature up to 11 RF I/Os per site, three RF sources with options for modulation, and one RF receiver per site. Vector and scalar network analysis is supported per site, with four site concurrent testing. A single instrument can also perform multi-site test with high efficiency enabled by the system DSP architecture. Devices such as RF mixers, synthesizers, LNAs, prescalers, Bluetooth™ wireless LAN transceivers, GSM, CDMA, W-CDMA, IQ transceivers, prescaler/charge pump, DECT devices, LNA/mixer/VCO, GPS chipset and IQ mod/demod are fully supported by the microwave instrument set, with tests including gain, IP3, noise figure, phase noise, 1dB compression, ACPR, EVM, and s-parameters. Each microwave instrument set contains its own general-purpose microprocessor with real-time operating system, providing local instrument control and DSP functions for all microwave measurements. Table 5-7 summarizes the key specifications for the Integra FLEX microwave instruments

FEATURE	SPECIFICATION
Frequency Range	50MHz to 6000MHz
Amplitude Range	+10dBm to –110dBm
Amplitude Resolution	0.1dB
Phase Noise	-150 dBc/Hz @ 2 GHz
Noise Floor	-161dBm/Hz
Modulation	2.7Ghz, 6Ghz
Frequency Hopping	100 microseconds

Table 5-7: Microwave instrument

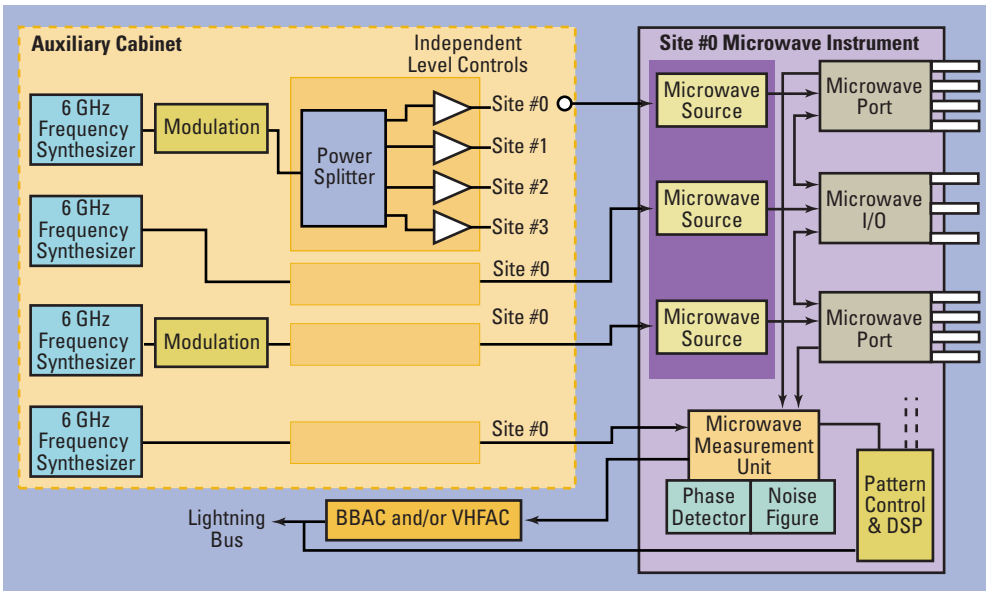


Figure 5-17: Microwave instrument block diagram

Precision Octal Opamp Loop (POOL) Instrument

POOL Instrument Feature	Specification	Accuracy
Op Amp Loop		
Range	20 V	
Bandwidth	100 KHz to 500 KHz	
Vol	10 µV	
Avol	140 dB	
Low Current Measurements		
Range	20 V	
Current Ranges		
Integrate	10 pA, 100 pA, 1 nA, 10 nA	
Resistive	100 nA, 1 µA, 10 µA	
12-Bit A/D Converter		
Sampling Rate	50 MHz	0.1 %
Ranges	10 V and 20 V	
Sample Memory	4 K samples	
16-Bit A/D Converter		
Sampling Rate	250 KHz	0.03 %
Ranges	10 V and 20 V	
Sample Memory	4 K samples	
Dual Event Time Stamper		
Ranges	10 V, Hi-Z	
Resolution	1 ns	±2 ns

Table 5-8: POOL instrument

The POOL instrument is a precision octal opamp loop designed to support multi-site testing of operational amplifiers. Each instrument provides eight (8) high precision op amp loop resources including dual picoamp ammeters, one 12-bit high speed A/D converter and one 16-bit high accuracy A/D converter, and a dual time stamper, all of which can be used as external instruments if needed. Shared resources on the POOL instrument consist of a 12-bit waveform generator, a 1,000 V/µs pulse generator, and pattern microcode support. Figure 5-18 illustrates the block diagram of the POOL instrument; Table 5-8 summarizes its key specifications.

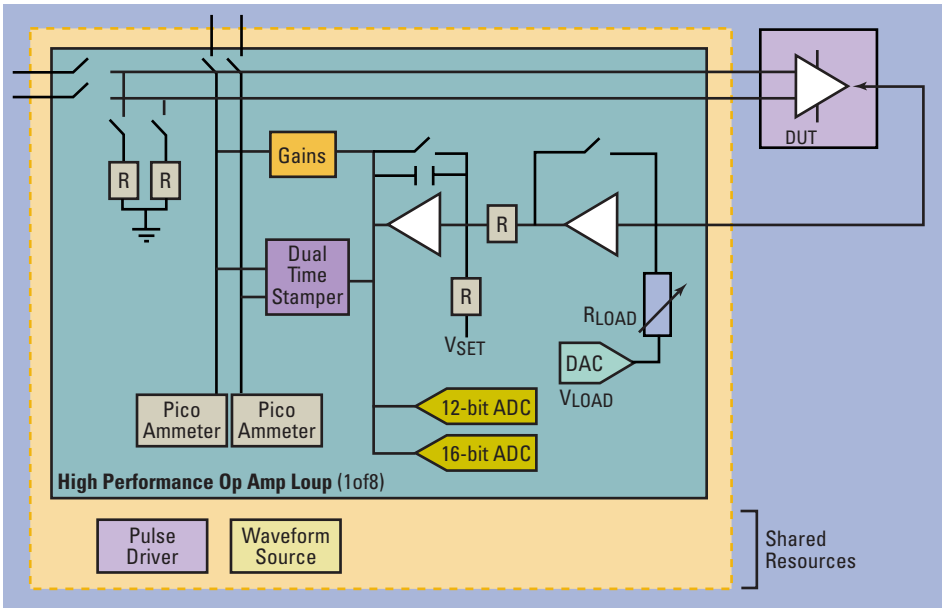


Figure 5-18: POOL instrument block diagram

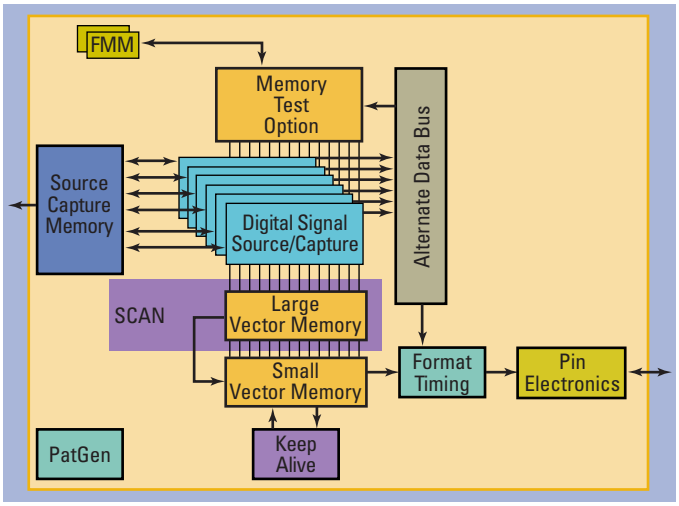


Figure 5-19: Digital instrument block diagram

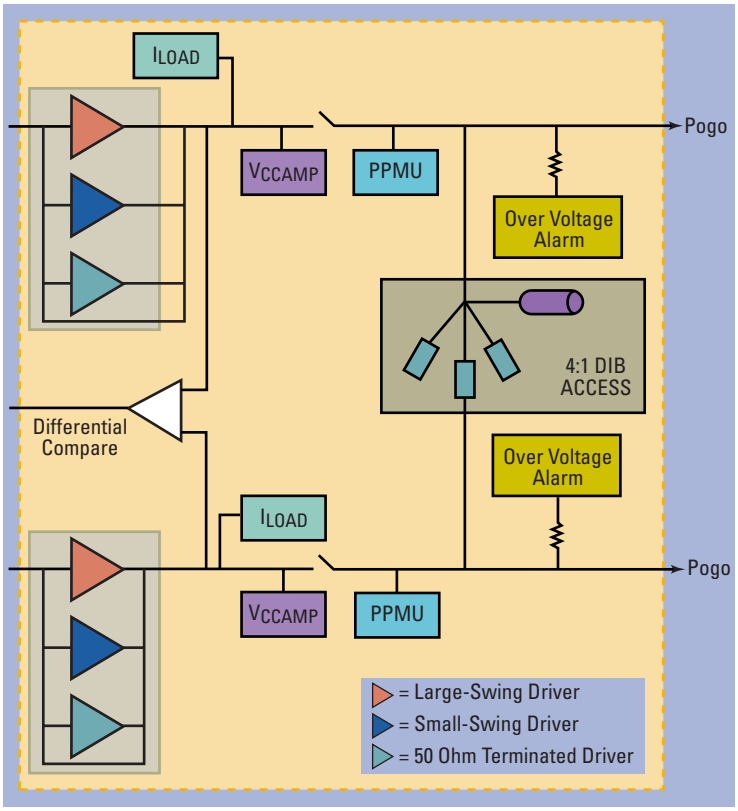


Figure 5-20: Integra FLEX pin electronics

General Capabilities

Integra FLEX digital instruments are based on the successful breakthrough in digital test economics of the J750 digital test system. Several features have been added that provide enhanced digital test capability, and allow the digital instruments to fully support multi-site DFT through mixed-signal SOC test applications on the Integra FLEX. Figure 5-19 depicts the overall block diagram of the digital instruments. Each section is described below.

Pin Electronics

Each digital instrument provides 48 single-ended pins/channels or 24 differential pin pairs, grouped in three blocks of 16 channels each. Each pin electronics channel provides three drivers — a large signal driver with a 500 mV to 5 V range and 10 mV accuracy, a small signal driver with a 50 mV to 500 mV range, 5 mV accuracy, and less than 600 ps rise time, a high speed 50 Ohm termination driver, a ±50 mA dynamic load, and a differential comparator with 500 MHz bandwidth. Refer to Figure 5-20.

Each pin is protected from overvoltage or overcurrent by an alarm circuit that disconnects the pin electronics from the DUT when an alarm condition is detected. Each pin has a dedicated PMU for parallel leakage and continuity testing. Two dedicated pins are provided with a high voltage (VIHH= 20 V) drive capability. A summary of key pin electronics features and specifications is provided in Table 5-9.

Digital Signal Source and Capture

The Digital Signal Source and Capture (DSSC) subsystem provides six (6) independent 16-bit Digital Signal Engines per instrument, each with an 8 MB x 16-bit memory. Each engine can be programmed to be source or capture, which allows up to six tests to occur simultaneously, at up to a 100 MHz data rate. Each pin can have up to 8 MB of digital waveform source or capture

memory behind it. Two engines can be grouped together to source or capture up to 32-bit wide parallel words. Virtual instruments can be configured by combining engines on a single board or across multiple boards. Serial or parallel instruments can coexist on the same board/instrument. Refer to Figure 5-21.

Table 5-10 illustrates how DSSC engines can be used for various source or capture modes at different PatGen frequencies and data widths.

Vector Memory

Vector memory for each pin in the Integra FLEX digital instrument consists of two blocks, a 64 MB Large Vector Memory (LVM) block, and a 1 KB Small Vector Memory (SVM) block. When patterns are compiled in the test program, the pattern vectors are stored in the LVM block for each pin, and the more complex opcodes such as loops, branches, device fail jumps, are stored in the SVM block. This memory assignment is transparent to the test engineer, and is handled by the test program. The LVM is reconfigured for use in SCAN testing to increase scan data memory to support a maximum scan chain depth of up to 1.5 G scan cycles. Refer to Figure 5-22.

Memory Test Option and Fail Map Memory

The Memory Test Option (MTO) is an on-board subsystem that generates address and data for testing of embedded memory functions at speeds up to 100 MHz. (Refer to Figures 5-23 and 5-24.) Each 48-pin digital instrument contains one (1) MTO subsystem, which can operate independently or synchronized with other MTO/instruments. Virtual MTO instruments can be configured that span multiple boards. Multiple MTO instruments can operate simultaneously. The MTO operates with a 1K or 2K vector instruction depth, depending on the overall operating mode of the Integra FLEX test system. Redundancy Analysis software is available which runs under the Auto-Smart DSP system. A summary of the features of the MTO are listed in Table 5-10.

The Fail Map Memory can be configured in a variety of depth and width options, and can support a number of modes:

- Build bit map on-the-fly from memory pattern data
- Build bit map off-line using memory pattern data stored in capture memory

Pin Electronics Feature	Specification	Accuracy
Large-Swing (Primary) Driver		
Quantity per instrument	48	
VIH/VIL Range	-1 to +6 V	±0.10% +14 mV
Programming Resolution	1 mV, typical	
Vt Range	-0.5 to +5.5 V	
DC Output Current	±50 mA	
Rise/Fall Time	600 ps, typical; 1 V swing	
High Voltage Driver		
Quantity per instrument	2, on dedicated pins	
VIHH		
Range	0 to +20 V	±100 mV
Programming Resolution	78 mV, typical	
Current		
Range	0 to +100 mA	±5 mA
Programming Resolution	0.5 mA, typical	
Current Sink	2.5 mA minimum	
Programmable Rise/Fall Time	1 to 16 µs	±0.5 µs
Small-Swing Driver		
VIH/VIL Range	50 to 500 mV	±0.10%
Programming Resolution	100 µV, typical	
Rise Time	500 ps, minimum; 100 mV swing	
Comparator		
VOH/VOL		
Range	-1 to +6 V	±0.10%
Programming Resolution	1 mV, typical	
Bandwidth	500 MHz, minimum	

Table 5-9: Pin electronics

DSSC Engine Usage Mode	Source or Capture PatGen Frequency	Data Width	Engines Used	Memory
Parallel	100 MHz	32	4	8Mword
Parallel	100 MHz	16	2	8Mword
Parallel	100 MHz	8	1	8Mword
Parallel	50 MHz	32	2	8Mword
Parallel	50 MHz	16	1	8Mword
Parallel	50 MHz	32	1	8Mword
Serial	100 MHz	32	1	4Mword
Serial	100 MHz	16	1	8Mword
Serial	50 MHz	32	1	4Mword
Serial	50 MHz	16	1	8Mword

Table 5-10: DSSC engine usage

- Build device map from device response
- Build accumulated and current fail map from device response
- Build bitmap using device response and expect data from memory pattern generator
- Build new fail map (mask mode) using device response and accumulated fail map (fail mask) from other map memory
- Source map data to memory pattern generator
- Source map data to other map memory
- Source compressed image to Capture Memory
- Capture Passes Only

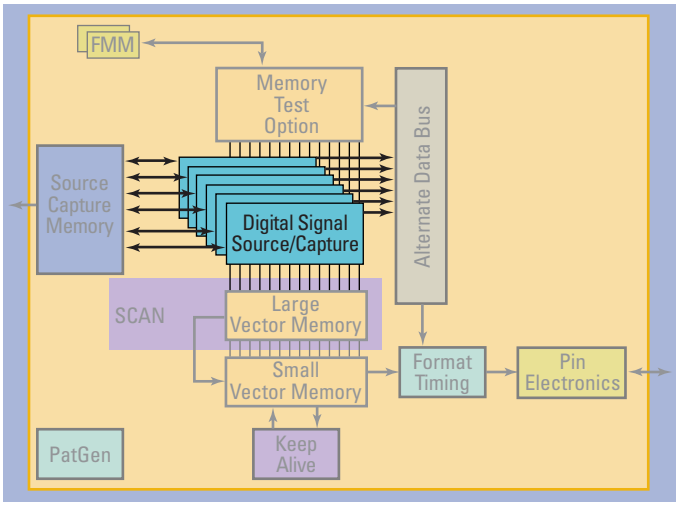


Figure 5-21: DSSC

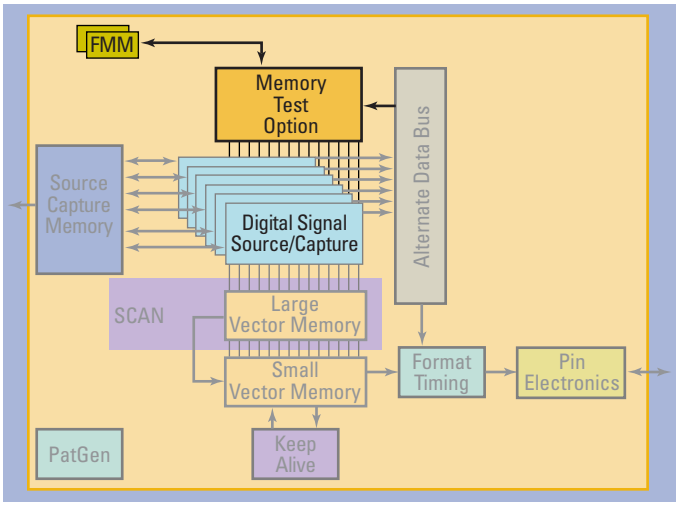


Figure 5-23: Memory test option

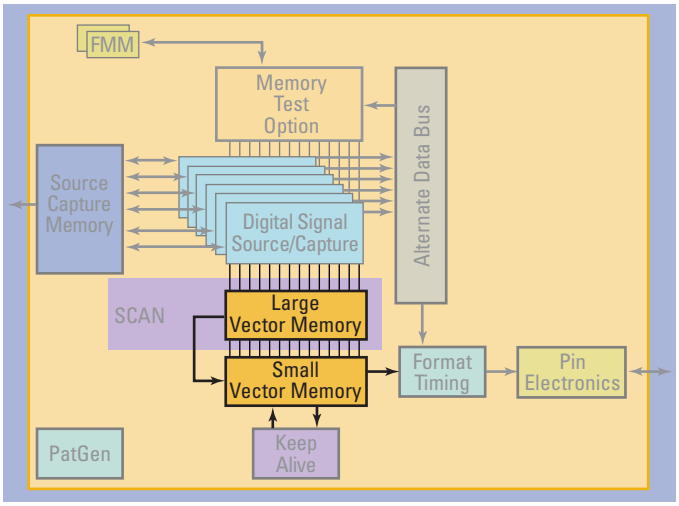


Figure 5-22: Vector Memory

SCAN

SCAN Flexibility and Speed

The optimal scan configuration will vary dramatically by device and package technology, DFT implementation, and test flow requirements. The Integra FLEX empowers the user with complete scan flexibility to optimize scan test strategy to specific needs, without loss of tester resources. Scan speed can run at up to 200 MHz for faster throughput and lower cost of test. Multiple scan channels can be configured as scan chains on the same digital instrument board or across multiple instrument boards. The number of scan chains is limited only by tester pin count, with maximum scan memory efficiency behind each chain. Each 16-channel scan instrument has 3Gbits of scan data memory available. This scan data can be allocated to a single channel or across all 16 channels, enabling the most efficient scan memory sharing. Scan data for each channel cycle can be 2 or 3 bits deep, and all channels can be configured for scan data to provide the required number of scan channels or scan depth. A continuous range of up to 24 scan chains is supported per 48-channel board (3x 16ch scan instruments per channel board). Refer to Figure 5-25.

SCAN Broadcast

The Integra FLEX's Alternate Data Bus architecture makes possible a breakthrough in DFT test economics and performance: the SCAN Broadcast capability. When testing multiple devices in parallel, SCAN Broadcast provides scan test patterns to each site from a single, shared scan data set pooled from the entire tester memory. SCAN Broadcast data is loaded once and fanned out to multiple sites driven from the same scan instrument. Each test site can "tune" to the SCAN Broadcast of the same copy of scan pattern data. This results in a doubling of SCAN memory available to each parallel test site, at no extra cost to the user. For example, if 8M scan memory is available to test a single site, keeping the same number of scan chains under a dual site configuration yields up to 16M for each site, without utilizing any memory upgrade. Four parallel sites yields a quadrupling to 32M of scan memory available, and so on. Refer to Figure 5-25.

Keep-Alive Function

The Keep-Alive function allows the digital instrument to provide a simple pattern to the DUT while the instrument is reconfigured for a subsequent test. Refer to Figure 5-26.

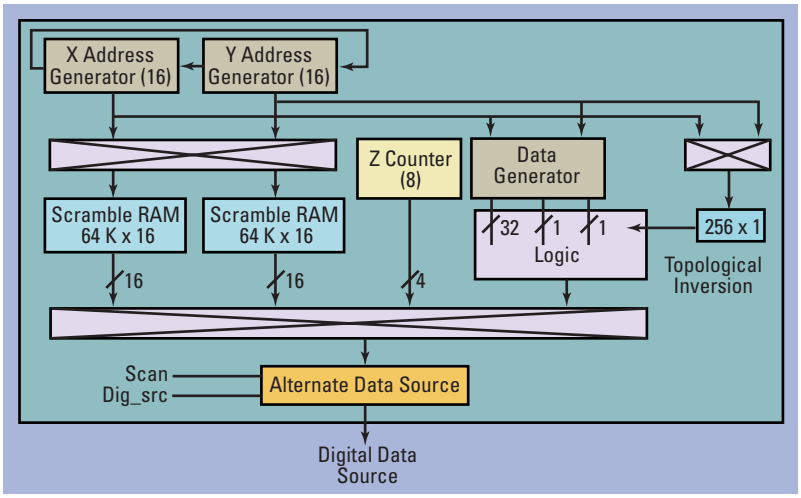
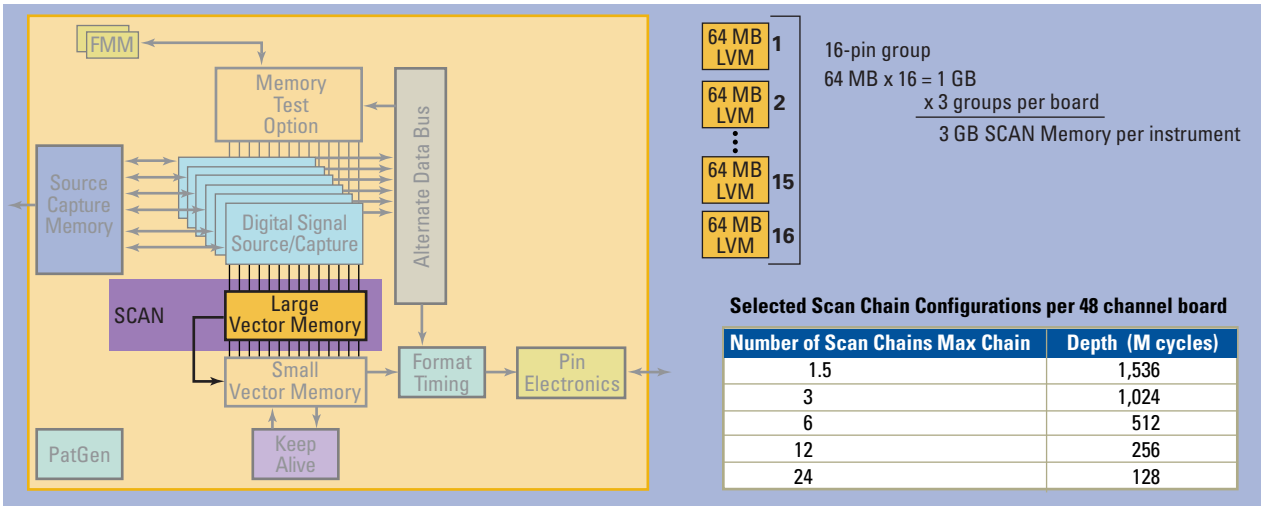


Figure 5-24: Memory test option detail

MTO Subsystem Features

Feature	Specification
MTO per Board/Instrument	1
Maximum Instruction Rate	100 M instructions/second
Address Generation	
X and Y Counter	16-bit
Z Counter	8-bit
Address Xcrambling	16-bit
Data Generation	
Width	32-bit
Data Generators	2, 1-bit or 1, 2-bit
Data Source	pattern memory or MTO generator on vector-by-vector basis
Topological Inversion	yes
Data Capture	
Capture Memory	24 M x 64-bit word sample (address and data) per board
Fail Map Memory	2 M x 32-bits
Utility Counters	
16-bit	2
32-bit	1

Table 5-10: MTO subsystem features



Selected Scan Chain Configurations per 48 channel board

Number of Scan Chains Max Chain	Depth (M cycles)
1.5	1,536
3	1,024
6	512
12	256
24	128

Figure 5-25: SCAN

From 1 to 16 vector sequences can be sourced in a loop. All failures can be masked during keep-alive, so accumulated fail can be valid across keep-alive boundaries. The Keep-Alive function will support modifications to the following features:

- All vector memories, LVM and SVM
- All channel timing values, i.e. edgesets
- The channel's TSET to edgeset mappings
- Period RAMs

The Keep-Alive function will not support modifications to pattern or tester modes (e.g. single to dual) or channel modes (e.g. normal to mux).

Alternate Data Bus

The Alternate Data Bus (ADB) provides a flexible and wide bus/crosspoint matrix function that allows MTO and DSSC resources to be routed to any of the 48 channels/pin electronics. The bus operates at a 50 MHz data rate; however multiplexing provides support for MTO and DSSC operation to 100 MHz. Refer to Figure 5-27.

Low-Jitter Clock Source — PicoClock Module

Clocks that will drive high-performance converters, modems, and data communications ICs must operate at both high frequency and low jitter, if clock noise is not

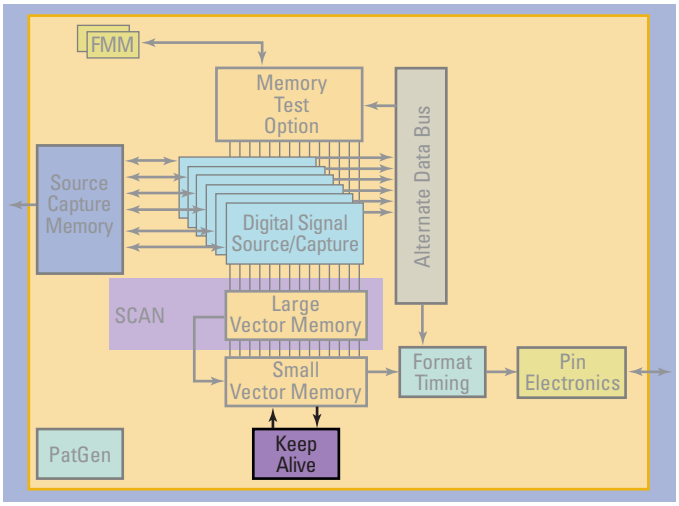


Figure 5-26: Keep-Alive

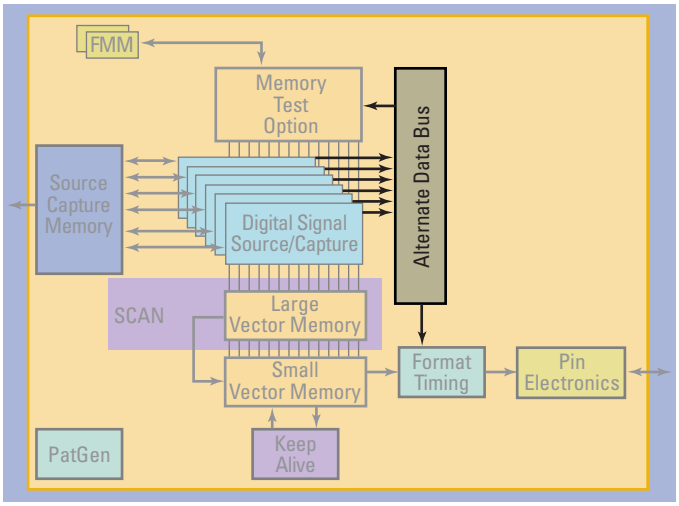


Figure 5-27: Alternate data bus

PicoClock Feature	Specification
Reference Input	
Frequency	≥5 MHz
Output	
Frequency	5 MHz to 1 GHz
Allowed Reference Multipliers/Output Frequency Range	
1 GHz to 500 MHz	2*(1, 2, … 100)
500 MHz to 250 MHz	1, 2, … 100
250 MHz to 5 MHz	1, 2, … 50
Drive	1.6 Vpp; differential PECL, centered on 3.9 V typical; note 1 and 2
Acquisition Time	< 4 ms for any size frequency change
Jitter (Note 3)	
960 MHz to >25 MHz	1.5 ps rms
25 MHz to >10 MHz	3.0 ps rms
10 MHz to 5 MHz	6.0 ps rms
Minimums Pulse Width	500 ps, nominal

Notes: 1. Nominal 50 Ohm termination in series with each complementary output.

2. The positive ECL logic levels are referenced to VCC=5.2 V.

3. All jitter within bandwidth from 100 Hz to Nyquist of clock rate or 40 MHz, whichever is lower, that is uncorrelated with system 10 MHz reference. Cycle to cycle rms jitter, locked on digital input reference channel.

Table 5-11: PicoClock

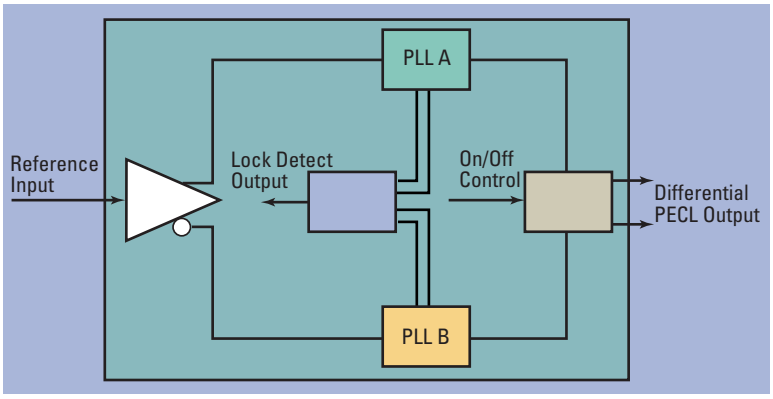


Figure 5-28: PicoClock block diagram

to affect test results or adversely impact test time. Each digital instrument can be configured with a low-jitter clock source — the PicoClock — which provides a 5 MHz to 1 GHz, 1.5 ps rms, ultra-low wideband jitter clock output.

Figure 5-28 depicts the block diagram of the PicoClock. The PicoClock accepts a reference input from any digital channel or analog source instrument through DIB Access. When driven by an analog instrument or controlled by second pattern generator, the PicoClock can run asynchronously to the system clock or the PatGen on the digital instrument on which the PicoClock is a subsystem. The reference input can range from 5.0 to 600 MHz, and is typically acquired in less than 500 µs. The reference input is multiplied by a user-specified integer, and output as a differential PECL clock signal. The duty cycle of the PicoClock output can be varied under program control. The output of the PicoClock can be gated ON/OFF under pattern control, without losing lock on the reference input. Simultaneous parametric testing of the DUT pins connected to both PicoClock outputs can be performed.

The Integra FLEX digital instruments can operate at a number of speeds, each enabled

as needed to match the test requirement and minimize cost of test. These speed points (please refer to *Section 2 – Meeting Test Floor Objectives*) are grouped into three operating mode categories — Single Mode, Dual Mode, and Quad Mode. The capabilities of these operating modes in terms of time sets and edge sets are described below. In general terms, within each operating mode, period, format, and timing can switch on-the-fly from one vector to the next. Edge placement accuracy is summarized in Table 5-12. Figure 5-29 provides a comparison of the overall mode timing.

Single Mode

The single mode (refer to Figure 5-30) operates at up to 50 MHz, with up to 256 Tsets and 32 Edgesets. Full SCAN, MTO, and DSSC operation, and single cycle I/O are supported. Vector depth is 64 Meg, with 3-bits per pin/vector. Six (6) edges — D0, D1, D2, D3, R1 and R2 — are available.

Dual Mode

The dual mode (refer to Figure 5-31) operates at up to 100 MHz, with up to 256 Tsets and 32 Edgesets. Full SCAN, MTO, and DSSC operation are supported. Vector depth is 64 Meg, with 3-bits per pin/vector. Five (5) edges — D0, D1, D2, D3, and R0 — in drive or receive cycles, as well as edge strobe are available.

Quad Mode

The quad mode (refer to Figure 5-32) operates at up to 200 MHz, with up to 64 Tsets and 16 Edgesets. Full SCAN, MTO, and DSSC operation are supported. Vector depth is 64 Meg, with 3-bits per pin/vector. Up to three (3) edges — D0, D1, and D2 in drive cycles, and D3 (if previous cycle is receive, and R0 in receive cycles, as well as edge strobe are available.

Edge Placement Accuracy Specification	Value
Clock Selection	Edges referenced to either T0 or C0 clock
Edge Range	
Single Mode	0 ns to (3*period – 20 ns)
Dual Mode	0 ns to (6*period – 20 ns)
Quad Mode	0 ns to (12*period – 20 ns)
Maximum Delay	10.24 µs
Edge Resolution	39.0625ps, nominal
Edge Placement Accuracy	
D1, D2, R0 (edge mode)	±250 ps
R1, R2 (window mode)	±500 ps
D0 (complement edge)	±250 ps
D0, D3 (HiZ, Terminate edges)	±500 ps
Overall Timing Accuracy	±354 ps; measured per SEMI G80-0200

Table 5-12: Edge placement accuracy

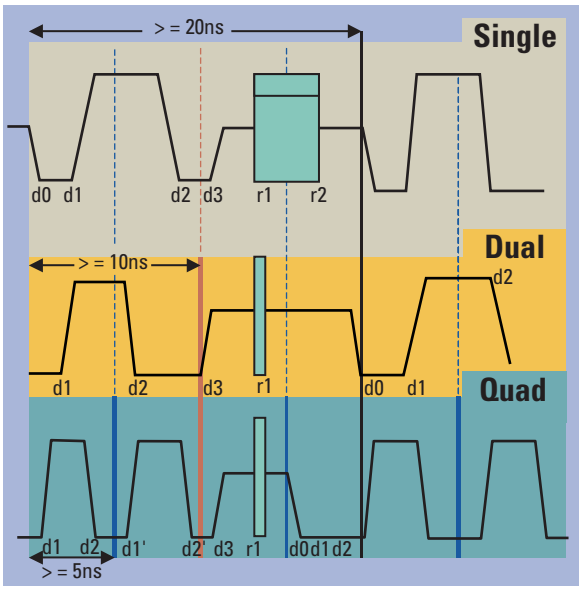


Figure 5-29: Mode comparison

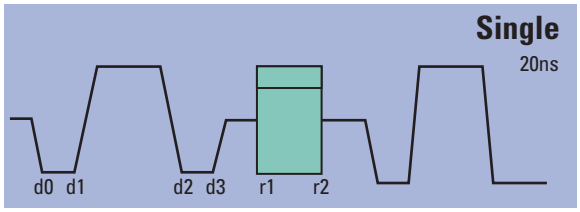


Figure 5-30: Single mode

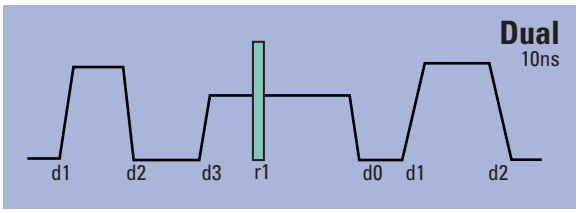


Figure 5-31: Dual mode

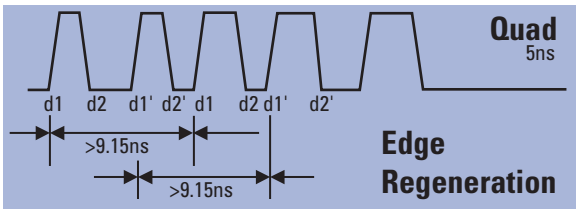


Figure 5-32: Quad mode

Appendix 1

Worldwide Support

Teradyne considers customer support equally as important as our test technology. Teradyne staffs applications and support centers worldwide that deliver innovative Operational and Engineering services, enabled by eSupport technologies, a description of which follows. A list of Teradyne sales offices is provided in Appendix 3.

Teradyne Test Assistance Group (TAG)

Recognized as the world's leading professional services organization for semiconductor device testers, Teradyne's Test Assistance Group (TAG) delivers Total Test Solutions worldwide. From design to high volume production, TAG's applications engineers are specialists in linear, mixed-signal, logic and memory testing devices. This value-added support includes test cell integration, test program and hardware development, tools for test productivity and skill development training. With more than 400 employees and 25 offices in 15 countries, TAG's global presence assures customers of a faster time to market for devices, increased test floor productivity and lower cost of test. A list of TAG offices and Technical Centers is provided in Appendix 3.

TAG provides value-added applications engineering support from design to volume production, delivering consistent, repeatable solutions to customers worldwide. At any phase of product testing and development, TAG's support will reduce your time to revenue and cost of test. We offer flexible agreements ranging from on-site engineering support to specific project assignments.

Test Program Development

For new devices, our engineers can develop or assist your engineering team in the development of a comprehensive test methodology and robust test plans. We develop complete test packages including test programs and interfacing hardware. We offer early stage device characterization as well as volume production solutions at wafer and final test. For existing devices TAG engineers can convert other system environments to the Teradyne platform, utilizing an internally developed library of program conversion tools and logic pattern converters resulting in faster time to market for new devices, and overall reductions in test development times.

Test Time Reduction (TTR)

Working closely with your team, TAG engineers will 1) identify the top volume devices for TTR work to provide the highest Return on Investment (ROI), and 2) modify test program software to reduce test time and minimize or eliminate a new qualification cycle. The direct benefits of higher throughput and better ROI can be realized immediately.

Yield Improvement

With appropriate test program modifications, improvements occur by tightening yield distribution against test limits as a result of better measurement accuracy. TAG can perform an in-depth analysis and modification of test programs and interface boards by assessing:

- test methodology
- tester instrument selection
- signal distribution to the Device Under Test (DUT)
- noise reduction techniques (higher sampling rates)

The direct benefit of reduced cost-of-test can be realized immediately.

Test Cell Integration

TAG engineers combine global production experience with specialized Teradyne tester knowledge to provide support in the following areas:

- assessment of current and future test cell requirements
- integration of key test cell components to the tester
- test programs transferred for new devices
- setup time reductions on handlers and probers
- program debug and data collection setup
- yield analysis and related interface problems
- tester up-time improvement by integrating with maintenance personnel
- network integration and administration

Direct benefits from increased test cell productivity, and reduced downtime, setup, and changeover times can all be realized.

Technical Consulting

Technical Consulting addresses production test issues beyond the scope of standard user documentation and training courses. TAG's engineers provide you access to our global organization's technical expertise, and will furnish:

- test process assessment, data collection and improvement recommendations
- CPK analysis to determine the vital test issues that affect your test cell performance

- solutions to software and hardware integration of handlers and probers
- rapid deployment of new device test programs to remote production facilities
- improve tester up-time by integrating with maintenance personnel

Teradyne's technical consulting services provide guidance on production test issues and strategic planning.

DocTool™

DocTool is a software tool for IMAGE™ that can automate the Test Package documentation for the Tiger platform, reducing development time as much as 75%. The resulting document, generated in HTML, is viewable from a standard web browser on any computer platform. In addition, DocTool's simplified graphical user interface allows the user to easily execute the various tasks required to create documentation.

DocTool's key features include:

- automatic detailed collection of test system hardware and software configuration
- dynamically captures IMAGE graphical test setup and DUT response
- allows custom documentation elements, for example, device and test specifications, DUT block diagram
- calculates and displays statistics on test results
- creates complete Test Package documentation in HTML format
- easy-to-use Test Package documentation browser with menus, clickable items and links to DocTool help
- conforms to internet standard formats
- simplified process for sharing and distributing test program documentation

Using DocTool, the majority of the main tasks necessary to create test documentation are performed automatically, including the capture of IMAGE debug tools windows, the insertion and layout of the various textual and graphical documentation elements, and the creation of a Table Of Contents. Test system time is only required to collect test results; most of the work is completed on the off-line IMAGE simulation (VX). DocTool provides up to a 75% reduction in Test Package documentation development time, with a documentation style and structure that are standardized across the company. Documentation is easily accessed on various computer platforms from local a directory or Intranet. DocTool enables test documentation development to become an integral part of the test program development workflow.

Interface Boards

Achieving optimal signal integrity is difficult as device speeds increase and more functionality is integrated on a single chip. Vital to the development process is the interface board design and fabrication. Both significantly impact the device program's introduction, which makes multiple interface board revisions unacceptable. With its unmatched understanding of key requirements for interfacing devices to the Teradyne test platform, TAG offers interface solutions for Wafer Probe, Manual Device and Automated Handler Device tests.

The Interface Products team is comprised of electrical engineers skilled in developing high performance test solutions. This expertise is essential to rapidly assessing and designing the interface board that will address critical signal path issues. The result is an increased probability that the board will work the first time, eliminating costly and time-consuming revisions. Our global network of 400 field applications engineers works with you to assess your requirements and ensure accuracy and responsiveness. Strict adherence to quality guidelines throughout the design and manufacturing process is maintained. In addition to standard continuity checks, as an option, Teradyne can perform functional tests on Teradyne testers at our manufacturing facility. Our Cadence Design Tools and a library of CAD conversion tools provide the flexibility to work with any CAD system. Because our team is experienced in a broad range of device technologies and mechanical interface requirements, TAG delivers expert advice on your interface board design. This consultation saves you both time and money.

Skills Development

For years, Teradyne's customers have benefited from the device test expertise of Test Assistance Group(TAG) engineers. This expertise, acknowledged by TAG's reputation as the leading professional services organization for semiconductor device testers, is continuously enhanced through up-to-date technical training and skill development courses, all of which are available for your engineers and technicians. Deployed globally in regional Technical Centers, TAG's technical training and skill development courses can also be delivered on site by TAG-certified instructors.

To develop, build and maintain up-to-date technical skills for customers, TAG organized its curriculum into three levels, i.e., ***Fundamentals of ATE***, ***User Programming***, and ***Advanced Seminars***. Each level builds on the previous level plus skill development attained on the job, further refining skills and bringing them to the next level. The ***Fundamentals of ATE*** courses provide a foundation in digital and mixed-signal test equipment with a focus on Teradyne systems. The ***User Programming*** courses build on the fundamentals courses and are Teradyne tester-specific. The ***Advanced Seminars*** concentrate on particular aspects of device specifications testing or Terdayne's tester instrumentation. In addition to these highly specialized training courses, TAG will, at your request, develop a customized Device/Tester/Job Function course specific to the needs of your engineers.

Teradyne Users Group (TUG)

The Teradyne Users Group (TUG) Conference was started by Teradyne customers in 1983. It is held each year at rotating locations within the U.S. This conference consists of technical papers, poster sessions and tutorials that present the latest in Test Technology. TUG is run by an annually elected steering committee of Teradyne customers with Teradyne appointed delegates. Sessions are available for a variety of Teradyne test systems and test issues, including:

Tiger/Catalyst/A5/VX sessions are for users who are interested in industry-leading SOC test systems.

- INTEGRA J750 sessions are for users of the INTEGRA J750, a highly integrated series of test systems designed for high parallel testing of devices in the low-end and mid-range semiconductor markets.
- Memory sessions are for users of highly parallel memory test systems, including the Probe-One, Marlin-J996 and the J990 Series.
- J9/VLSI sessions are for users of J973-Series and J971-Series High-Performance VLSI Test Systems.
- MFT (Manufacturing Functional Test) sessions are for users whose interests encompass areas traditionally referred to as FBT (Functional Board Test). Test engineers involved in developing, architecting, or maintaining functional board test program sets will want to attend.
- MPT sessions, (Manufacturing Process Test), encompass areas historically classed as ICT, (In Circuit Test) as well as Optical Inspection systems (AOI). These sessions should be of interest to any engineers involved in monitoring the quality of circuit boards as they move through a production process.

Attendance at the annual TUG conference has grown over the years, from 20 enthusiastic customers at the first meeting in Boston, to over 900 attendees in San Diego in 2000. In addition to the U.S. conference, the European board test customers meet annually for an ETUG conference, and Teradyne's Japan office hosts a one day Mini-TUG for the Semiconductor products.

eSupport

eSupport is a suite of products that enable Teradyne's customers to obtain self-service, as well as assisted support. Currently, eSupport products include the eKnowledge portal, eConnect NET, and the Customer Care Center. eSupport products are integrated into Teradyne service agreements, enhancing the current support that Teradyne provides to its customers.

eKnowledge Portal

The eKnowledge Portal is a technical support website that provides 24x7 self-service access to solutions, documents, and technical assistance. Customers can submit requests for assistance online, and can then track the status of their requests from beginning to resolution. This new, more efficient method of managing incidents ensures that customers receive faster responses to their requests for assistance. Before solutions are made available through the eKnowledge portal, they are verified for accuracy, as well as reviewed for customer-specific information. The eKnowledge portal will be available in 2002.

eConnect NET

eConnect NET is a secure eDiagnostics solution that provides remote control and operation of test systems, enabling Teradyne engineers worldwide to collaborate with you on engineering and maintenance issues. eConnect NET provides multiple layers of security, controlled by both Teradyne and the customer, ensuring that only authorized Teradyne employees have the ability to access specific, approved machines. eConnect NET is currently available in some areas, and plans are underway to make it available worldwide. Teradyne provides training to customers who use eConnect NET.

Customer Care Center

The Customer Care Center provides live telephone assistance for technical support, parts, and training.

Appendix 2

Contacting Teradyne

Sales Offices

BOSTON AREA

Bedford, MA
Integra Test Division
Manufacturing, Sales, and Service

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Kneeland St.
Administration

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North Reading, MA
ATD Manufacturing

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Nashua, NH
Connector Assembly
Teradyne Connection Systems Division
Teradyne Connection Systems Inc.

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Memory Test & VLSI Test Manufacturing, Foundry West Manufacturing

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Building 4

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Building 5

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Dana Point, CA
Backplane Systems and Assemblies

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Irvine, CA
Sales for Circuit Board, Mixed Signal, VLSI, Memory, Broadband Test

Applications Support for Mixed Signal, VLSI, Memory Test

Sales, Applications and Maintenance Support for Broadband Test

Aerospace & Defense Sales for Backplane Systems and Interconnects

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